intel

394-129

# D27128
# 128K (16K x 8) UV ERASABLE PROM

- 250 ns Maximum Access Time . . . HMOS*-E Technology
- Compatible with High-Speed 8 MHz iAPX 186...Zero WAIT State
- Two-Line Control
- Pin Compatible to 2764 EPROM
- Industry Standard Pinout . . . JEDEC Approved
- ±10% $V_{CC}$ Tolerance Available
- Low Active Current . . . 100 mA Max.
- inteligent Programming™ Algorithm

The Intel 27128 is a 5V only, 131,072-bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The standard 27128 access time is 250 ns which is compatible with high-performance microprocessors such as Intel's 8 MHz iAPX 186. In these systems the 27128 allows the microprocessor to operate without the addition of WAIT states. The 27128 is also compatible with the 12 MHz 8051 family.

An important 27128 feature is the separate output control, Output Enable ($\overline{OE}$) from the Chip Enable control ($\overline{CE}$). The $\overline{OE}$ control eliminates bus contention in microprocessor systems. Intel's Application Note AP-72 describes the microprocessor system implementation of the $\overline{OE}$ and $\overline{CE}$ controls on Intel's EPROMs. AP-72 is available from Intel's Literature Department.

The 27128 has standby mode which reduces the power consumption without increasing access time. The maximum active current is 100 mA, while the maximum standby current is only 40 mA. The standby mode is selected by applying a TTL-high signal to the $\overline{CE}$ input.

±10% $V_{CC}$ tolerance is available as an alternative to the standard ±5% $V_{CC}$ tolerance for the 27128. This can allow the system designer more leeway with regard to his power supply requirements and other system parameters.

The 27128 is fabricated with HMOS*-E technology, Intel's high-speed N-channel MOS Silicon Gate Technology.

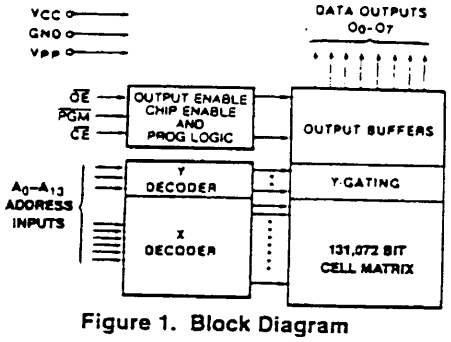
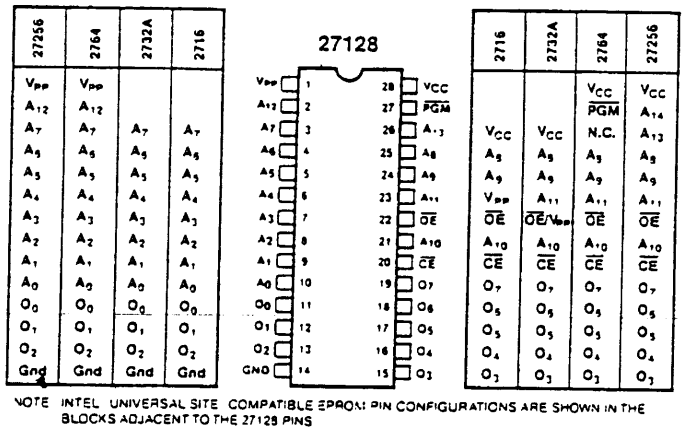



Figure 1. Block Diagram




NOTE: INTEL UNIVERSAL SITE COMPATIBLE EPROM PIN CONFIGURATIONS ARE SHOWN IN THE BLOCKS ADJACENT TO THE 27128 PINS

Figure 2. Pin Configurations

## MODE SELECTION

| Mode \ Pins | $\overline{CE}$ (20) | $\overline{OE}$ (22) | $\overline{PGM}$ (27) | $A_9$ (24) | $V_{PP}$ (1) | $V_{CC}$ (28) | Outputs (11-13, 15-19) |
|---|---|---|---|---|---|---|---|
| Read | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | X | $V_{CC}$ | $V_{CC}$ | $D_{OUT}$ |
| Output Disable | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | X | $V_{CC}$ | $V_{PP}$ | High Z |
| Standby | $V_{IH}$ | X | X | X | $V_{CC}$ | $V_{CC}$ | High Z |
| Program | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | X | $V_{PP}$ | $V_{CC}$ | $D_{IN}$ |
| Verify | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | X | $V_{PP}$ | $V_{CC}$ | $D_{OUT}$ |
| Program Inhibit | $V_{IH}$ | X | X | X | $V_{PP}$ | $V_{CC}$ | High Z |
| Intelligent Identifier | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_H$ | $V_{CC}$ | $V_{CC}$ | Code |
| Intelligent Programming | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | X | $V_{PP}$ | $V_{CC}$ | $D_{IN}$ |

NOTES:
1. X can be $V_{IH}$ or $V_{IL}$
2. $V_H$ = 12.0V ± 0.5V

## PIN NAMES

| | |
|---|---|
| $A_0$-$A_{13}$ | ADDRESSES |
| $\overline{CE}$ | CHIP ENABLE |
| $\overline{OE}$ | OUTPUT ENABLE |
| $O_0$-$O_7$ | OUTPUTS |
| $\overline{PGM}$ | PROGRAM |
| N.C. | NO CONNECT |

*HMOS is a patented process of Intel Corporation.



FEBRUARY 1983
ORDER NUMBER: 210224-004

## ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... −10°C to +80°C
Storage Temperature ..... −65°C to +125°C
All Input or Output Voltages with Respect to Ground ..... +7.0V to −0.6V
Voltage on Pin 24 with Respect to Ground ..... +13.5V to −0.6V
$V_{PP}$ Supply Voltage with Respect to Ground During Programming ..... +22V to −0.6V

*NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## D.C. AND A.C. OPERATING CONDITIONS DURING READ

| | 27128 | 27128-3 | 27128-4 | 27128-25 | 27128-30 | 27128-45 |
|---|---|---|---|---|---|---|
| Operating Temperature Range | 0°C–70°C | 0°C–70°C | 0°C–70°C | 0°C–70°C | 0°C–70°C | 0°C–70°C |
| $V_{CC}$ Power Supply[1,2] | 5V ± 5% | 5V ± 5% | 5V ± 5% | 5V ± 10% | 5V ± 10% | 5V ± 10% |
| $V_{PP}$ Voltage[2] | $V_{PP} = V_{CC}$ | $V_{PP} = V_{CC}$ | $V_{PP} = V_{CC}$ | $V_{PP} = V_{CC}$ | $V_{PP} = V_{CC}$ | $V_{PP} = V_{CC}$ |

## READ OPERATION

### D.C. CHARACTERISTICS

| Symbol | Parameter | Limits | | | Units | Test Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ.[3] | Max | | |
| $I_{LI}$ | Input Load Current | | | 10 | µA | $V_{IN} = 5.5V$ |
| $I_{LO}$ | Output Leakage Current | | | 10 | µA | $V_{OUT} = 5.5V$ |
| $I_{PP1}$[2] | $V_{PP}$ Current Read/Standby | | | 5 | mA | $V_{PP} = 5.5V$ |
| $I_{CC1}$[2] | $V_{CC}$ Current Standby | | 15 | 40 | mA | $\overline{CE} = V_{IH}$ |
| $I_{CC2}$[2] | $V_{CC}$ Current Active | | 60 | 100 | mA | $\overline{CE} = \overline{OE} = V_{IL}$ |
| $V_{IL}$ | Input Low Voltage | −.1 | | −.8 | V | |
| $V_{IH}$ | Input High Voltage | 2.0 | | $V_{CC}+1$ | V | |
| $V_{OL}$ | Output Low Voltage | | | .45 | V | $I_{OL} = 2.1$ mA |
| $V_{OH}$ | Output High Voltage | 2.4 | | | V | $I_{OH} = -400$ µA |

### A.C. CHARACTERISTICS

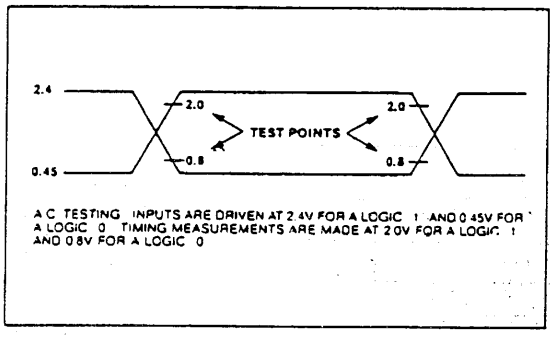
| Symbol | Parameter | 27128-25 & 27128 Limits | | 27128-30 & 27128-3 Limits | | 27128-45 & 27128-4 Limits | | Units | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| $t_{ACC}$ | Address to Output Delay | | 250 | | 300 | | 450 | ns | $\overline{CE} = \overline{OE} = V_{IL}$ |
| $t_{CE}$ | $\overline{CE}$ to Output Delay | | 250 | | 300 | | 450 | ns | $\overline{OE} = V_{IL}$ |
| $t_{OE}$ | $\overline{OE}$ to Output Delay | | 100 | | 120 | | 150 | ns | $\overline{CE} = V_{IL}$ |
| $t_{DF}$[4] | $\overline{OE}$ High to Output Float | 0 | 60 | 0 | 105 | 0 | 130 | ns | $\overline{CE} = V_{IL}$ |
| $t_{OH}$ | Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First | 0 | | 0 | | 0 | | ns | $\overline{CE} = \overline{OE} = V_{IL}$ |

NOTES:
1. $V_{CC}$ must be applied simultaneously or before $V_{PP}$ and removed simultaneously or after $V_{PP}$.
2. $V_{PP}$ may be connected directly to $V_{CC}$ except during programming. The supply current would then be the sum of $I_{CC}$ and $I_{PP1}$.
3. Typical values are for $t_A = 25°C$ and nominal supply voltages.
4. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram on page 3.

## CAPACITANCE ($T_A$ = 25°C, f = 1 MHz)

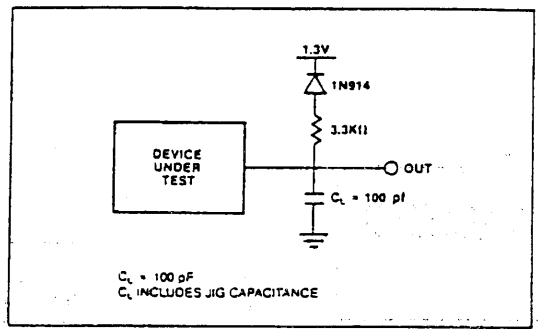
| Symbol | Parameter | Typ.[1] | Max. | Unit | Conditions |
|---|---|---|---|---|---|
| $C_{IN}$[2] | Input Capacitance | 4 | 6 | pF | $V_{IN}$ = 0V |
| $C_{OUT}$ | Output Capacitance | 8 | 12 | pF | $V_{OUT}$ = 0V |

## A.C. TESTING INPUT/OUTPUT WAVEFORM



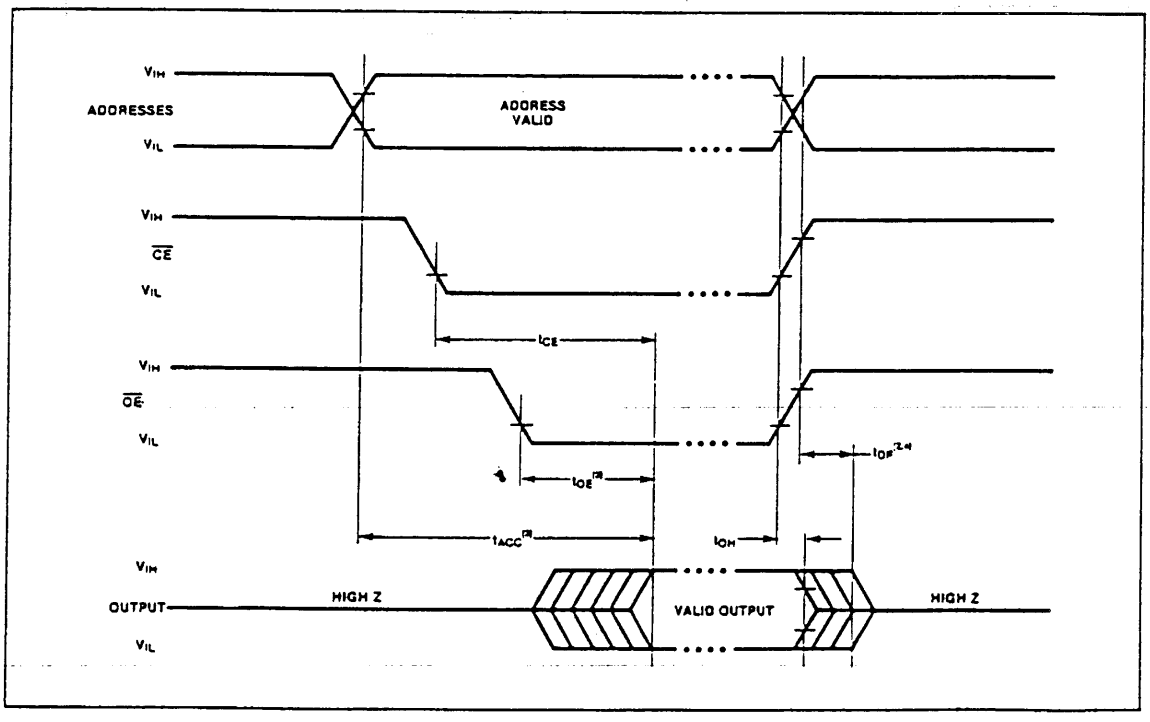

A.C. TESTING INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.45V FOR A LOGIC "0". TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0".

## A.C. TESTING LOAD CIRCUIT




$C_L$ = 100 pF
$C_L$ INCLUDES JIG CAPACITANCE

## A.C. WAVEFORMS




**NOTES:**
1. Typical values are for $T_A$ = 25°C and nominal supply voltages.
2. This parameter is only sampled and is not 100% tested.
3. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on $t_{ACC}$.
4. $t_{DF}$ is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

## STANDARD PROGRAMMING

**D.C. PROGRAMMING CHARACTERISTICS:** $T_A = 25 \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 21V \pm 0.5V$ (see Note 1)

| Symbol | Parameter | Limits | | | Test Conditions |
|---|---|---|---|---|---|
| | | Min. | Max. | Unit | |
| $I_{LI}$ | Input Current (All Inputs) | | 10 | μA | $V_{IN} = V_{IL}$ or $V_{IH}$ |
| $V_{OL}$ | Output Low Voltage During Verify | | 0.45 | V | $I_{OL} = 2.1$ mA |
| $V_{OH}$ | Output High Voltage During Verify | 2.4 | | V | $I_{OH} = -400$ μA |
| $V_{IL}$ | Input Low Level (All Inputs) | -0.1 | 0.8 | V | |
| $V_{IH}$ | Input High Level | 2.0 | $V_{CC} + 1$ | V | |
| $I_{CC1}$ | $V_{CC}$ Supply Current (Program Inhibit) | | 40 | mA | $\overline{CE} = V_{IH}$ |
| $I_{CC2}$ | $V_{CC}$ Supply Current (Program & Verify) | | 100 | mA | |
| $I_{PP2}$ | $V_{PP}$ Supply Current (Program) | | 30 | mA | $\overline{CE} = V_{IL} = \overline{PGM}$ |
| $I_{PP3}$ | $V_{PP}$ Supply Current (Verify) | | 5 | mA | $\overline{CE} = V_{IL}$ $\overline{PGM} = V_{IH}$ |
| $I_{PP4}$ | $V_{PP}$ Supply Current (Program Inhibit) | | 5 | mA | $\overline{CE} = V_{IH}$ |
| $V_{ID}$ | Ag Inteligent Identifier Voltage | 11.5 | 12.5 | V | |

**A.C. PROGRAMMING CHARACTERISTICS:** $T_A = 25 \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 21V \pm 0.5V$ (see Note 1)

| Symbol | Parameter | Limits | | | | Test Conditions* |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Unit | |
| $t_{AS}$ | Address Setup Time | 2 | | | μs | |
| $t_{OES}$ | $\overline{OE}$ Setup Time | 2 | | | μs | |
| $t_{DS}$ | Data Setup Time | 2 | | | μs | |
| $t_{AH}$ | Address Hold Time | 0 | | | μs | |
| $t_{DH}$ | Data Hold Time | 2 | | | μs | |
| $t_{DFP}$[2] | Output Enable to Output Float Delay | 0 | | 130 | ns | |
| $t_{VS}$ | $V_{PP}$ Setup Time | 2 | | | μs | |
| $t_{PW}$ | $\overline{PGM}$ Pulse Width During Programming | 45 | 50 | 55 | ms | |
| $t_{CES}$ | $\overline{CE}$ Setup Time | 2 | | | μs | |
| $t_{OE}$ | Data Valid from $\overline{OE}$ | | | 150 | ns | |

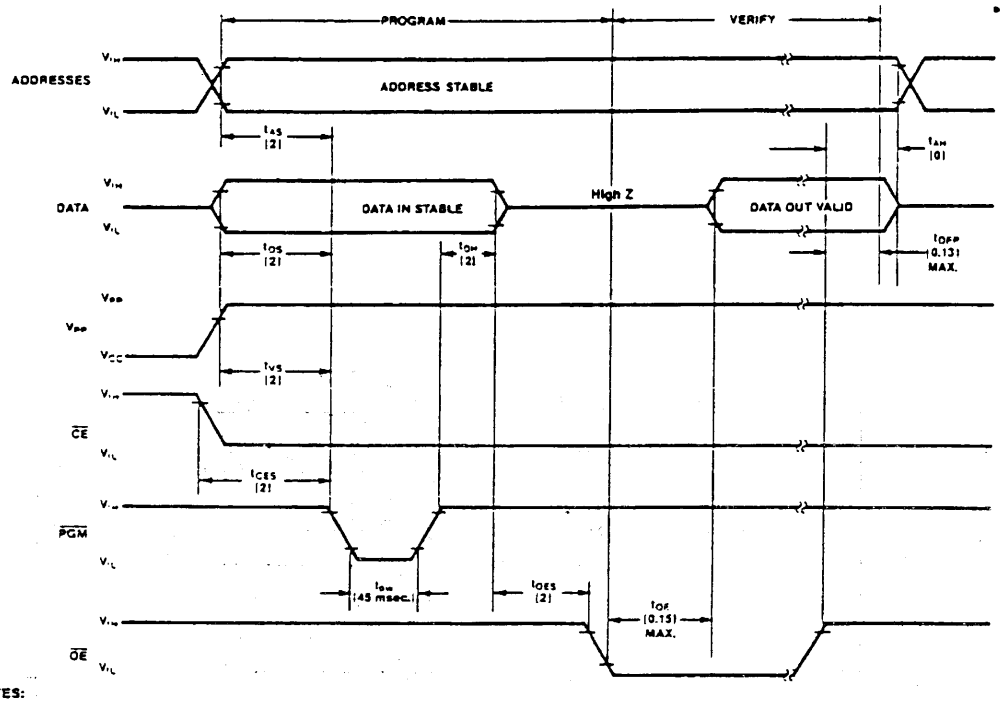
***A.C. CONDITIONS OF TEST**

Input Rise and Fall Times (10% to 90%) ..... 20 ns
Input Pulse Levels ..... 0.45V to 2.4V
Input Timing Reference Level ..... 0.8V and 2.0V
Output Timing Reference Level ..... 0.8V and 2.0V

**NOTES:**

1. $V_{CC}$ must be applied simultaneously or before $V_{PP}$ and removed simultaneously or after $V_{PP}$.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram on page 5.

## STANDARD PROGRAMMING WAVEFORMS




NOTES:
1. ALL TIMES SHOWN IN [ ] ARE MINIMUM AND IN μSEC UNLESS OTHERWISE SPECIFIED.
2. THE INPUT TIMING REFERENCE LEVEL IS .8V FOR A $V_{IL}$ AND 2V FOR A $V_{IH}$.
3. $t_{OE}$ AND $t_{OFP}$ ARE CHARACTERISTICS OF THE DEVICE BUT MUST BE ACCOMMODATED BY THE PROGRAMMER.
4. WHEN PROGRAMMING THE 27128, A 0.1μF CAPACITOR IS REQUIRED ACROSS $V_{PP}$ AND GROUND TO SUPRESS SPURIOUS VOLTAGE TRANSIENTS WHICH CAN DAMAGE THE DEVICE.

## ERASURE CHARACTERISTICS

The erasure characteristics of the 27128 are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000 Å range. Data show that constant exposure to room level fluorescent lighting could erase the typical 27128 in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the 27128 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the 27128 window to prevent unintentional erasure.

The recommended erasure procedure for the 27128 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15 Wsec/cm². The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm² power rating. The 27128 should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose a 27128 can be exposed to without damage is 7258 Wsec/cm² (1 week @ 12000 μW/cm²). Exposure of the 27128 to high intensity UV light for long periods may cause permanent damage.

## DEVICE OPERATION

The eight modes of operation of the 27128 are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for $V_{PP}$ and 12V on A9 for int$_e$ligent Identifier mode.

**Table 1. Mode Selection**

| Mode \ Pins | $\overline{CE}$ (20) | $\overline{OE}$ (22) | $\overline{PGM}$ (27) | $A_9$ (24) | $V_{PP}$ (1) | $V_{CC}$ (28) | Outputs (11–13, 15–19) |
|---|---|---|---|---|---|---|---|
| Read | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | X | $V_{CC}$ | $V_{CC}$ | $D_{OUT}$ |
| Output Disable | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | X | $V_{CC}$ | $V_{CC}$ | High Z |
| Standby | $V_{IH}$ | X | X | X | $V_{CC}$ | $V_{CC}$ | High Z |
| Program | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | X | $V_{PP}$ | $V_{CC}$ | $D_{IN}$ |
| Verify | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | X | $V_{PP}$ | $V_{CC}$ | $D_{OUT}$ |
| Program Inhibit | $V_{IH}$ | X | X | X | $V_{PP}$ | $V_{CC}$ | High Z |
| int$_e$ligent Identifier | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_H$ | $V_{CC}$ | $V_{CC}$ | Code |
| int$_e$ligent Programming | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | X | $V_{PP}$ | $V_{CC}$ | $D_{IN}$ |

NOTES:
1. X can be $V_{IH}$ or $V_{IL}$
2. $V_H$ = 12.0V ±0.5V

## READ MODE

The 27128 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins, independent of device selection. Assuming that addresses are stable, the address access time ($t_{ACC}$) is equal to the delay from $\overline{CE}$ to output ($t_{CE}$). Data is available at the outputs after a delay of $t_{OE}$ from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

## STANDBY MODE

The 27128 has standby mode which reduces the maximum active current from 100 mA to 40 mA. The 27128 is placed in the standby mode by applying a TTL-high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

### Output OR-Tieing

Because EPROMs are usually used in larger memory arrays, Intel has provided 2 control lines which accommodate this multiple memory connection. The two control lines allow for:

a) the lowest possible memory power dissipation, and
b) complete assurance that output bus contention will not occur.

To use these two control lines most efficiently, $\overline{CE}$ (pin 20) should be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 22) should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are active only when data is desired from a particular memory device.

### System Considerations

The power switching characteristics of HMOS-E EPROMs require careful decoupling of the devices. The supply current, $I_{CC}$, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by the falling and rising edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitive loading of the device. The associated transient voltage peaks can be suppressed by complying with Intel's Two-Line Control, as detailed in Intel's Application Note, AP-72, and by properly selected decoupling capacitors. It is recommended that a 0.1 $\mu$F ceramic capacitor be used on every device between $V_{CC}$ and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 $\mu$F bulk electrolytic capacitor should be used between $V_{CC}$ and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage droop caused by the inductive effects of PC board traces.

## PROGRAMMING MODES

***Caution: Exceeding 22V on pin 1 ($V_{PP}$) will permanently damage the 27128.***

Initially, and after each erasure, all bits of the 27128 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The 27128 is in the programming mode when $V_{PP}$ input is at 21V and $\overline{CE}$ and $\overline{PGM}$ are both at TTL low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

### Standard Programming

For programming, $\overline{CE}$ should be kept TTL-low at all times while $V_{PP}$ is kept at 21V. When the address and data are stable, a 50 msec, active-low, TTL program pulse is applied to the $\overline{PGM}$ input. A program pulse must be applied at each address location to be programmed. You can program any location at any time —either individually, sequentially, or at random. The program pulse has a maximum width of 55 msec.

Programming of multiple 27128s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled 27128s may be connected together when they are programmed with the same data. A low-level TTL pulse applied to the $\overline{PGM}$ input programs the paralleled 27128s.

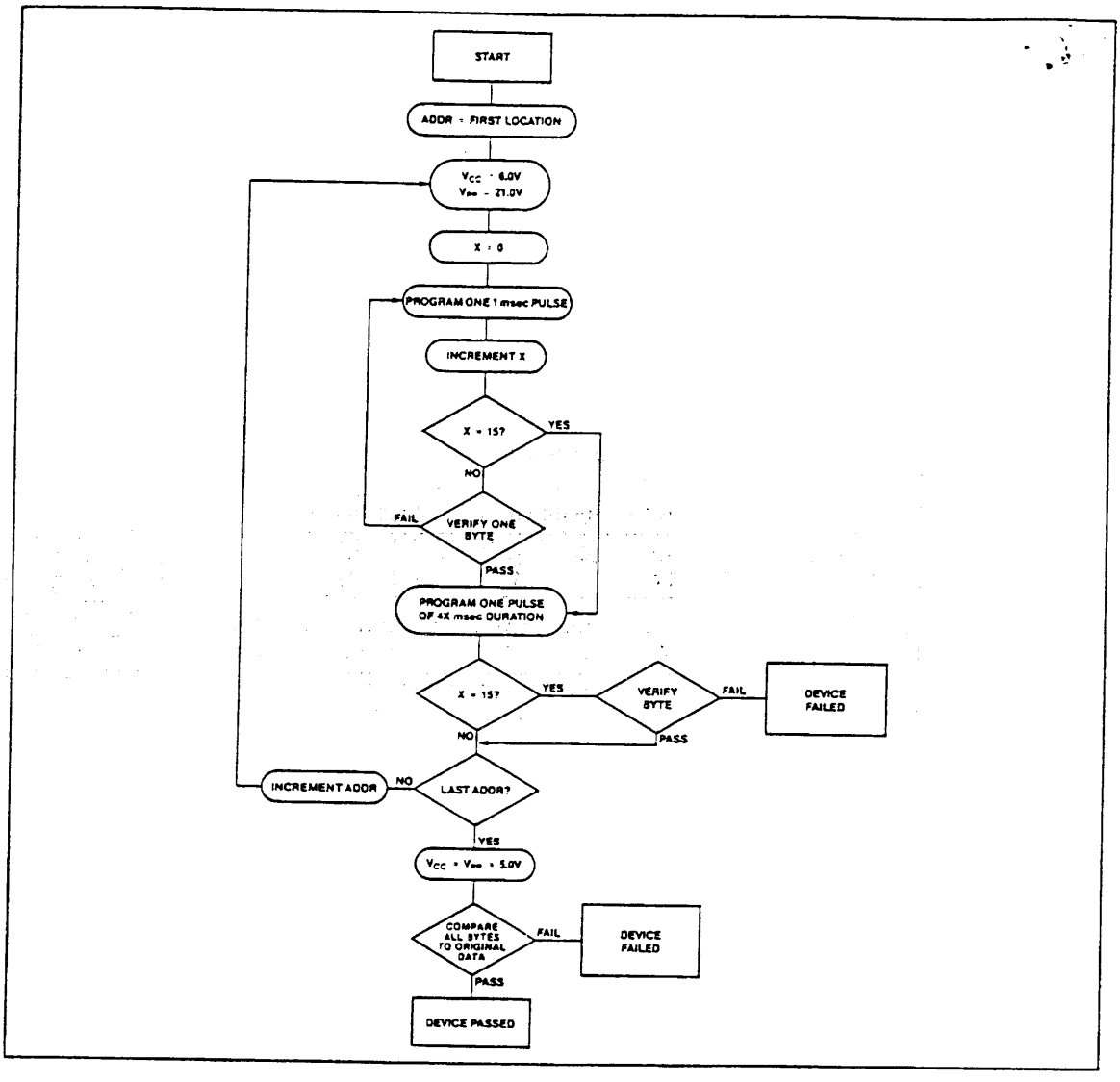



**Figure 3. 27128 int$_e$ligent Programming™ Flowchart**

## Program Inhibit

Programming of multiple 27128s in parallel with different data is easily accomplished by using the Program Inhibit mode. A high-level $\overline{CE}$ or $\overline{PGM}$ input inhibits the other 27128s from being programmed. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel 27128s may be common. A TTL low-level pulse applied to the $\overline{CE}$ and $\overline{PGM}$ inputs with $V_{PP}$ at 21V will program the selected 27128.

## Verify

A verify should be performed on the programmed bits to determine that they have been correctly programmed. The verify is performed with $\overline{CE}$ and $\overline{OE}$ at $V_{IL}$, $\overline{PGM}$ at $V_{IH}$ and $V_{PP}$ at 21V.

## int$_e$ligent Programming™ Algorithm

The 27128 int$_e$ligent Programming Algorithm allows Intel 27128s to be programmed in a significantly faster time than the standard 50 msec per byte programming routine. Typical programming times for 27128s are on the order of two minutes, which is a six-fold reduction in programming time from the standard method. This fast algorithm results in the same reliability characteristics as the standard 50 msec algorithm. A flowchart of the 27128 int$_e$ligent

Programming Algorithm is shown in Figure 3. This is compatible with the 2764 int$_e$ligent Programming Algorithm.

With the standard programming method, data is programmed into a selected 27128 location by a single 50 msec, active-low, TTL pulse applied to the $\overline{PGM}$ pin. The int$_e$ligent Programming Algorithm utilizes two different pulse types: initial and overprogram. The duration of the initial $\overline{PGM}$ pulse(s) is one millisecond, which will then be followed by a longer overprogram pulse of length 4X msec. X is an iteration counter and is equal to the number of the initial one millisecond pulses applied to a particular 27128 location, before a correct verify occurs. Up to 15 one-millisecond pulses per byte are provided for before the overprogram pulse is applied.

***The entire sequence of program pulses and byte verifications is performed at $V_{CC}$ = 6.0V and $V_{PP}$ = 21.0V.*** When the int$_e$ligent Programming cycle has been completed, all bytes should be compared to the original data with $V_{CC} = V_{PP} = 5.0V$.

## int$_e$ligent Programming™ Algorithm

**D.C. PROGRAMMING CHARACTERISTICS:** $T_A = 25 \pm 5°C$, $V_{CC} = 6.0V \pm 0.25V$, $V_{PP} = 21V \pm 0.5V$

| Symbol | Parameter | Limits | | | Test Conditions (see Note 1) |
|---|---|---|---|---|---|
| | | Min. | Max. | Unit | |
| $I_{LI}$ | Input Current (All Inputs) | | 10 | μA | $V_{IN} = V_{IL}$ or $V_{IH}$ |
| $V_{IL}$ | Input Low Level (All Inputs) | -0.1 | 0.8 | V | |
| $V_{IH}$ | Input High Level | 2.0 | $V_{CC}+1$ | V | |
| $V_{OL}$ | Output Low Voltage During Verify | | 0.45 | V | $I_{OL}$ = 2.1 mA |
| $V_{OH}$ | Output High Voltage During Verify | 2.4 | | V | $I_{OH}$ = -400 μA |
| $I_{CC2}$ | $V_{CC}$ Supply Current (Program & Verify) | | 100 | mA | |
| $I_{PP2}$ | $V_{PP}$ Supply Current (Program) | | 30 | mA | $\overline{CE} = V_{IL} = \overline{PGM}$ |
| $V_{ID}$ | A$_9$ int$_e$ligent Identifier Voltage | 11.5 | 12.5 | V | |

**A.C. PROGRAMMING CHARACTERISTICS:** $T_A = 25 \pm 5°C$, $V_{CC} = 6.0V \pm 0.25V$, $V_{PP} = 21V \pm 0.5V$

| Symbol | Parameter | Limits | | | | Test Conditions* (see Note 1) |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Unit | |
| $t_{AS}$ | Address Setup Time | 2 | | | μs | |
| $t_{OES}$ | $\overline{OE}$ Setup Time | 2 | | | μs | |
| $t_{DS}$ | Data Setup Time | 2 | | | μs | |
| $t_{AH}$ | Address Hold Time | 0 | | | μs | |
| $t_{DH}$ | Data Hold Time | 2 | | | μs | |
| $t_{DFP}$[4] | Output Enable to Output Float Delay | 0 | | 130 | ns | |
| $t_{VPS}$ | $V_{PP}$ Setup Time | 2 | | | μs | |
| $t_{VCS}$ | $V_{CC}$ Setup Time | 2 | | | μs | |
| $t_{PW}$ | $\overline{PGM}$ Initial Program Pulse Width | 0.95 | 1.0 | 1.05 | ms | (see Note 3) |
| $t_{OPW}$ | $\overline{PGM}$ Overprogram Pulse Width | 3.8 | | 63 | ms | (see Note 2) |
| $t_{CES}$ | $\overline{CE}$ Setup Time | 2 | | | μs | |
| $t_{OE}$ | Data Valid from $\overline{OE}$ | | | 150 | ns | |

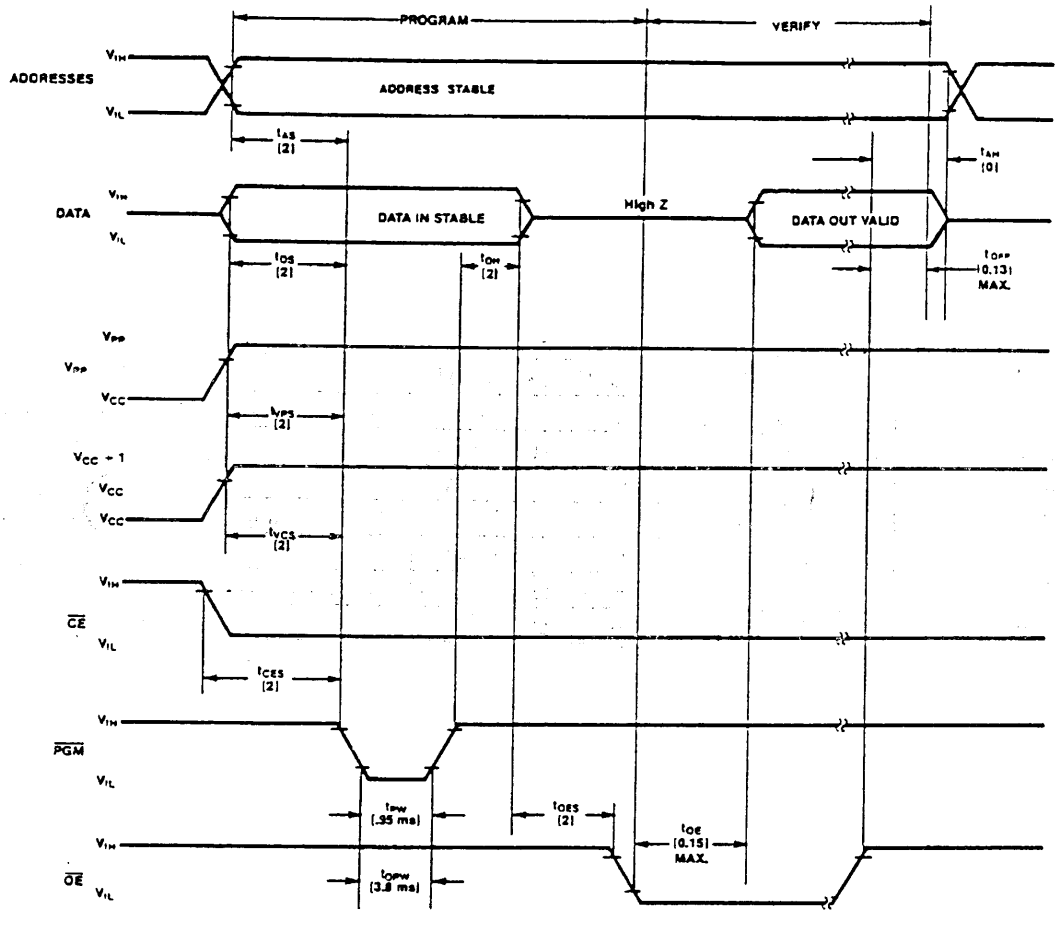
***A.C. CONDITIONS OF TEST**

Input Rise and Fall Times (10% to 90%) ..... 20 ns
Input Pulse Levels ..... 0.45V to 2.4V
Input Timing Reference Level ..... 0.8V and 2.0V
Output Timing Reference Level ..... 0.8V and 2.0V

**NOTES:**

1. $V_{CC}$ must be applied simultaneously or before $V_{PP}$ and removed simultaneously or after $V_{PP}$.
2. The length of the overprogram pulse will vary from 3.8 msec to 63 msec as a function of the iteration counter value X.
3. Initial Program Pulse width tolerance is 1 msec ± 5%.
4. This parameter is only sampled as is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram on page 9.

## inteligent Programming™ WAVEFORMS




NOTES:
1. ALL TIMES SHOWN IN [ ] ARE MINIMUM AND IN μSEC UNLESS OTHERWISE SPECIFIED.
2. THE INPUT TIMING REFERENCE LEVEL IS .8V FOR A $V_{IL}$ AND 2V FOR A $V_{IH}$.
3. $t_{OE}$ AND $t_{DFP}$ ARE CHARACTERISTICS OF THE DEVICE BUT MUST BE ACCOMMODATED BY THE PROGRAMMER.
4. WHEN PROGRAMMING THE 27128, A 0.1μF CAPACITOR IS REQUIRED ACROSS $V_{PP}$ AND GROUND TO SUPRESS SPURIOUS VOLTAGE TRANSIENTS WHICH CAN DAMAGE THE DEVICE.

## inteligent Identifier™ Mode

The inteligent Identifier Mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range.

To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 (pin 24) of the 27128. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 (pin 10) from $V_{IL}$ to $V_{IH}$. All other address lines must be held at $V_{IL}$ during inteligent Identifier Mode.

Byte 0 (A0 = $V_{IL}$) represents the manufacturer code and byte 1 (A0 = $V_{IH}$) the device identifier code. For the Intel 27128, these two identifier bytes are given in Table 2. All identifiers for manufacturer and device codes will possess odd parity, with the MSB ($O_7$) defined as the parity bit.

Intel will begin manufacturing 27128s during 1982 that will contain the inteligent Identifier feature. Earlier generation devices will not contain identifier information, and if erased, will respond with a "one" ($V_{OH}$) on each data line when operated in this mode. Programmed, pre-identifier mode 27128s will respond with the current data contained in locations 0 and 1 when subjected to the inteligent Identifier operation.

**Table 2. 27128 inteligent Identifier Bytes**

| Identifier \ Pins | $A_0$ (10) | $O_7$ (19) | $O_6$ (18) | $O_5$ (17) | $O_4$ (16) | $O_3$ (15) | $O_2$ (13) | $O_1$ (12) | $O_0$ (11) | Hex Data |
|---|---|---|---|---|---|---|---|---|---|---|
| Manufacturer Code | $V_{IL}$ | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 89 |
| Device Code | $V_{IH}$ | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 83 |