MCM4116B

16,384-BIT DYNAMIC RANDOM ACCESS MEMORY

The MCM4116B is a 16,384-bit, high-speed dynamic Random Access Memory designed for high-performance, low-cost applications in mainframe and buffer memories and peripheral storage. Organized as 16,384 one-bit words and fabricated using Motorola's highly reliable N-channel double-polysilicon technology, this device optimizes speed, power, and density tradeoffs.

By multiplexing row and column address inputs, the MCM4116B requires only seven address lines and permits packaging in Motorola's standard 16-pin dual in-line packages. This packaging technique allows high system density and is compatible with widely available automated test and insertion equipment. Complete address decoding is done on chip with address latches incorporated.

All inputs are TTL compatible, and the output is 3-state TTL compatible. The data output of the MCM4116B is controlled by the column address strobe and remains valid from access time until the column address strobe returns to the high state. This output scheme allows higher degrees of system design flexibility such as common input/output operation and two dimensional memory selection by decoding both row address and column address strobes.

The MCM4116B incorporates a one-transistor cell design and dynamic storage techniques, with each of the 128 row addresses requiring a refresh cycle every 2 milliseconds.

- Flexible Timing with Read-Modify-Write, RAS-Only Refresh, and Page-Mode Capability
- Industry Standard 16-Pin Package
- 16,384 X 1 Organization
- ±10% Tolerance on All Power Supplies
- All Inputs are Fully TTL Compatible
- Three-State Fully TTL-Compatible Output
- Common I/O Capability When Using "Early Write" Mode
- On-Chip Latches for Addresses and Data In
- Low Power Dissipation — 463 mW Active, 20 mW Standby (Max)
- Fast Access Time Options: 150 ns — MCM4116BP-15, BC-15
  200 ns — MCM4116BP-20, BC-20
  250 ns — MCM4116BP-25, BC-25
  300 ns — MCM4116BP-30, BC-30
- Easy Upgrade from 16-Pin 4K RAMs

ABSOLUTE MAXIMUM RATINGS (See Note)

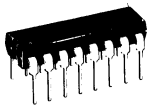
Rating	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{BB}	V_{in}, V_{out}	-0.5 to +20	V
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Power Dissipation	P_D	1.0	W
Data Out Current	I_{out}	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

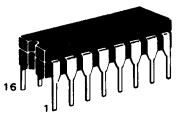
MOS

(N-CHANNEL)

16,384-BIT DYNAMIC RANDOM ACCESS MEMORY

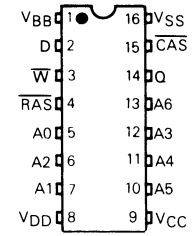


P SUFFIX
PLASTIC PACKAGE
CASE 648



C SUFFIX
FRIT-SEAL CERAMIC PACKAGE
CASE 620

PIN ASSIGNMENT

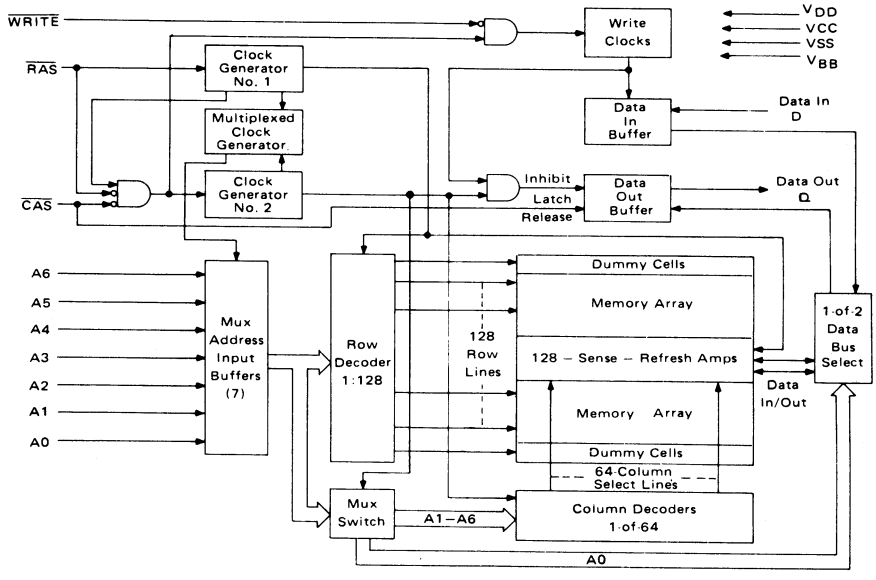


PIN NAMES	
A0-A6	Address Inputs
CAS	Column Address Strobe
D	Data In
Q	Data Out
RAS	Row Address Strobe
W	Read/Write Input
V_{BB}	Power (−5 V)
V_{CC}	Power (+5 V)
V_{DD}	Power (+12 V)
V_{SS}	Ground

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

DS9806/10-79

BLOCK DIAGRAM



DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	V_{DD}	10.8	12.0	13.2	V	1
	V_{CC}	4.5	5.0	5.5	V	1, 2
	V_{SS}	0	0	0	V	1
	V_{BB}	-4.5	-5.0	-5.5	V	1
Logic 1 Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	V_{IHC}	2.4	–	7.0	V	1
Logic 1 Voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	V_{IH}	2.4	–	7.0	V	1
Logic 0 Voltage, all inputs	V_{IL}	-1.0	–	0.8	V	1

DC CHARACTERISTICS (V_{DD} = 12 V ±10%, V_{CC} = 5.0 V ±10%, V_{BB} = -5.0 V ±10%, V_{SS} = 0 V, T_A = 0 to 70°C.)

Characteristic	Symbol	Min	Max	Units	Notes
Average V_{DD} Power Supply Current	I_{DD1}	–	35	mA	4
V_{CC} Power Supply Current	I_{CC}	–	–	mA	5
Average V_{BB} Power Supply Current	$I_{BB1,3}$	–	200	µA	
Standby V_{BB} Power Supply Current	I_{BB2}	–	100	µA	
Standby V_{DD} Power Supply Current	I_{DD2}	–	1.5	mA	6
Average V_{DD} Power Supply Current during "$\overline{RAS}$ only" cycles	I_{DD3}	–	27	mA	4
Input Leakage Current (any input)	$I_{I(L)}$	–	10	µA	
Output Leakage Current	$I_{O(L)}$	–	10	µA	6, 7
Output Logic 1 Voltage @ I_{out} = -5 mA	V_{OH}	2.4	–	V	2
Output Logic 0 Voltage @ I_{out} = 4.2 mA	V_{OL}	–	0.4	V	

NOTES:

1. All voltages referenced to V_{SS}. V_{BB} must be applied before and removed after other supply voltages.
2. Output voltage will swing from V_{SS} to V_{CC} under open circuit conditions. For purposes of maintaining data in power-down mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations. V_{OH}(min) specification is not guaranteed in this mode.
3. Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate.
4. Current is proportional to cycle rate; maximum current is measured at the fastest cycle rate.
5. I_{CC} depends upon output loading. The V_{CC} supply is connected to the output buffer only.
6. Output is disabled (open-circuit) when $\overline{CAS}$ is at a logic 1.
7. $0 V \leq V_{out} \leq +5.5 V$.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, periodically sampled rather than 100% tested) (See Note 8)

Parameter	Symbol	Typ	Max	Unit	Notes
Input Capacitance (A0-A5), D_{in}	C_{I1}	4.0	5.0	pF	9
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	C_{I2}	8.0	10	pF	9
Output Capacitance (D_{out})	C_o	5.0	7.0	pF	7, 9

AC OPERATING CONDITIONS AND CHARACTERISTICS (See Notes 3, 9, 14)

READ, WRITE, AND READ-MODIFY-WRITE CYCLES

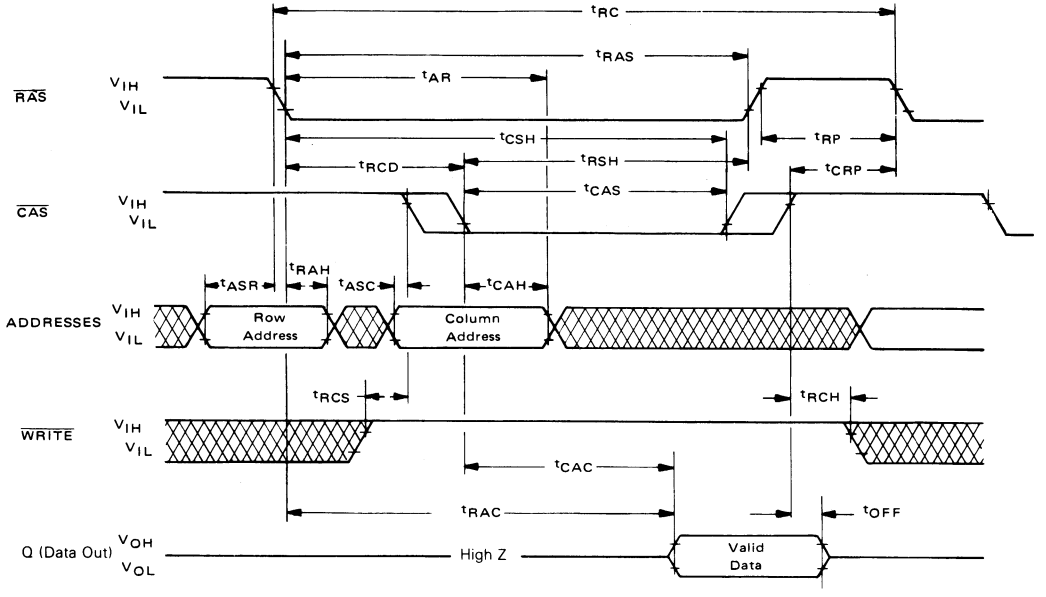
(V_{DD} = 12 V ±10%, V_{CC} = 5.0 V ±10%, V_{BB} = −5.0 V ±10%, V_{SS} = 0 V, T_A = 0 to 70°C.)

Parameter	Symbol	MCM4116B-15		MCM4116B-20		MCM4116B-25		MCM4116B-30		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	375	–	375	–	410	–	480	–	ns	
Read Write Cycle Time	t_{RWC}	375	–	375	–	515	–	660	–	ns	
Access Time from Row Address Strobe	t_{RAC}	–	150	–	200	–	250	–	300	ns	10, 12
Access Time from Column Address Strobe	t_{CAC}	–	100	–	135	–	165	–	200	ns	11, 12
Output Buffer and Turn-off Delay	t_{OFF}	0	50	0	50	0	60	0	60	ns	17
Row Address Strobe Precharge Time	t_{RP}	100	–	120	–	150	–	180	–	ns	
Row Address Strobe Pulse Width	t_{RAS}	150	10,000	200	10,000	250	10,000	300	10,000	ns	
Column Address Strobe Pulse Width	t_{CAS}	100	10,000	135	10,000	165	10,000	200	10,000	ns	
Row to Column Strobe Lead Time	t_{RCD}	20	50	25	65	35	85	60	100	ns	13
Row Address Setup Time	t_{ASR}	0	–	0	–	0	–	0	–	ns	
Row Address Hold Time	t_{RAH}	20	–	25	–	35	–	60	–	ns	
Column Address Setup Time	t_{ASC}	−10	–	−10	–	−10	–	−10	–	ns	
Column Address Hold Time	t_{CAH}	45	–	55	–	75	–	100	–	ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{AR}	95	–	120	–	160	–	200	–	ns	
Transition Time (Rise and Fall)	t_T	3.0	35	3.0	50	3.0	50	3.0	50	ns	14
Read Command Setup Time	t_{RCS}	0	–	0	–	0	–	0	–	ns	
Read Command Hold Time	t_{RCH}	0	–	0	–	0	–	0	–	ns	
Write Command Hold Time	t_{WCH}	45	–	55	–	75	–	100	–	ns	
Write Command Hold Time Referenced to $\overline{RAS}$	t_{WCR}	95	–	120	–	160	–	200	–	ns	
Write Command Pulse Width	t_{WP}	45	–	55	–	75	–	100	–	ns	
Write Command to Row Strobe Lead Time	t_{RWL}	60	–	80	–	100	–	180	–	ns	
Write Command to Column Strobe Lead Time	t_{CWL}	60	–	80	–	100	–	180	–	ns	
Data in Setup Time	t_{DS}	0	–	0	–	0	–	0	–	ns	15
Data in Hold Time	t_{DH}	45	–	55	–	75	–	100	–	ns	15
Data in Hold Time Referenced to $\overline{RAS}$	t_{DHR}	95	–	120	–	160	–	200	–	ns	
Column to Row Strobe Precharge Time	t_{CRP}	−20	–	−20	–	−20	–	−20	–	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	100	–	135	–	165	–	200	–	ns	
Refresh Period	t_{RFSH}	–	2.0	–	2.0	–	2.0	–	2.0	ms	
$\overline{WRITE}$ Command Setup Time	t_{WCS}	−20	–	−20	–	−20	–	−20	–	ns	
$\overline{CAS}$ to $\overline{WRITE}$ Delay	t_{CWD}	70	–	95	–	125	–	180	–	ns	16
$\overline{RAS}$ to $\overline{WRITE}$ Delay	t_{RWD}	120	–	160	–	210	–	280	–	ns	16
$\overline{CAS}$ Precharge Time (Page mode cycle only)	t_{CP}	60	–	80	–	100	–	100	–	ns	
Page Mode Cycle Time	t_{PC}	170	–	225	–	275	–	325	–	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	150	–	200	–	250	–	300	–	ns	

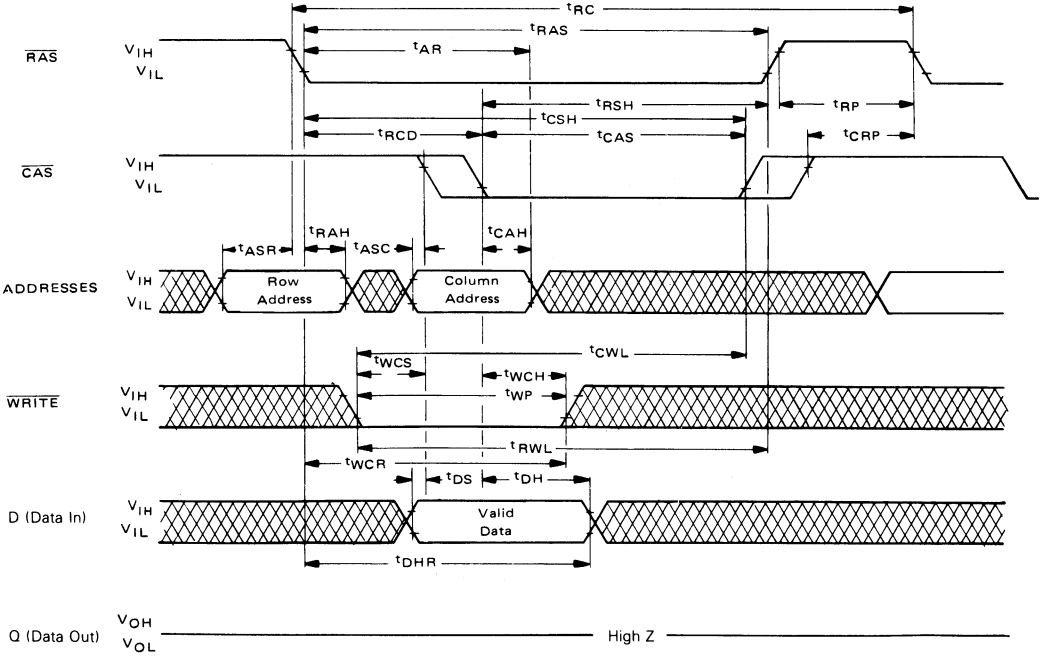
NOTES: (continued)

8. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = \frac{I\Delta_t}{\Delta V}$.
9. AC measurements assume t_T = 5.0 ns.
10. Assumes that $t_{RCD} + t_T \leq t_{RCD}$ (max).
11. Assumes that $t_{RCD} + t_T \geq t_{RCD}$ (max).
12. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
13. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
14. V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transistion times are measured between V_{IHC} or V_{IH} and V_{IL}.
15. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.
16. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell; If neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
17. Assumes that $t_{CRP} > 50$ ns.

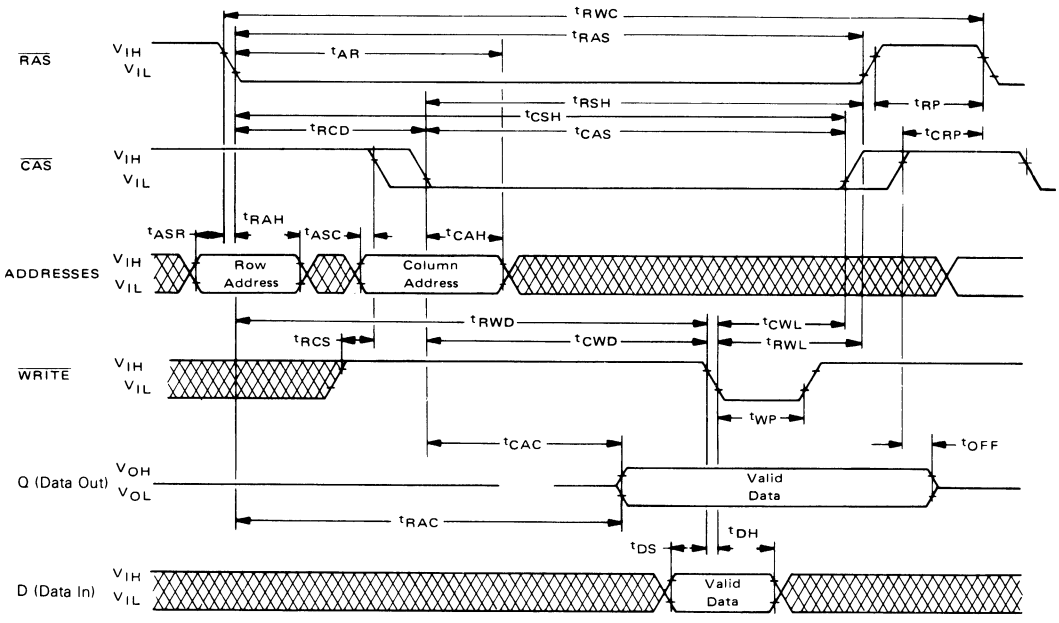
READ CYCLE TIMING



WRITE CYCLE TIMING

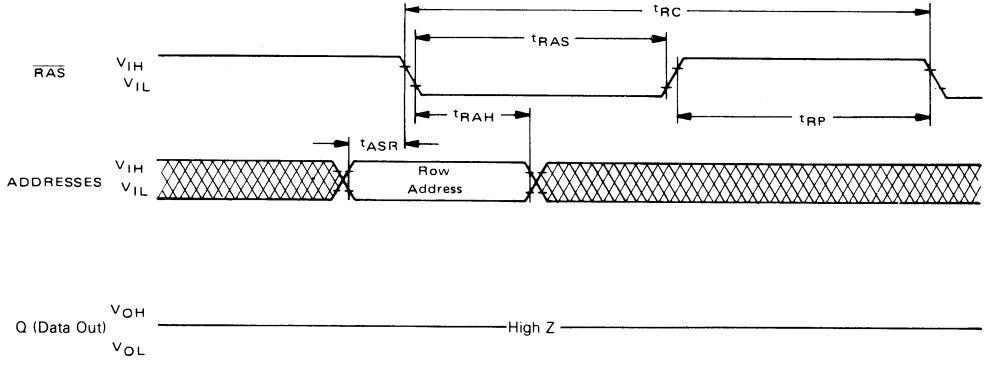


READ-WRITE/READ-MODIFY-WRITE CYCLE

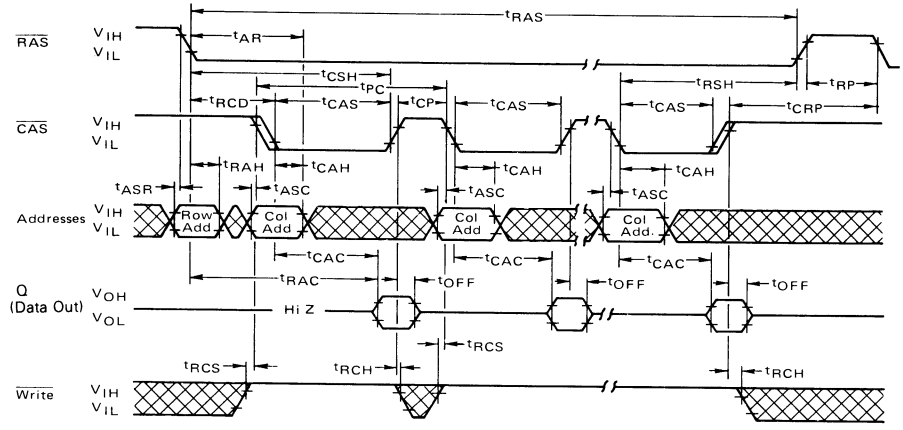


RAS ONLY REFRESH TIMING

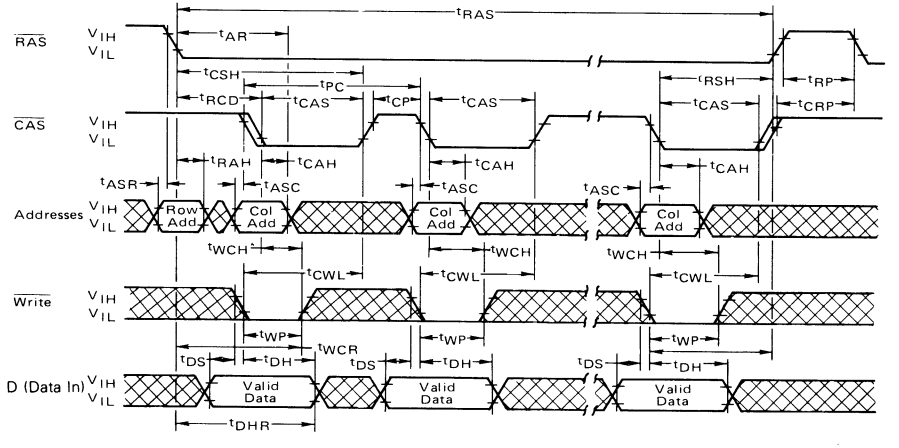
Note: $\overline{CAS}$ = V_{IHC}, $\overline{WRITE}$ = Don't Care



PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



MCM4116B BIT ADDRESS MAP