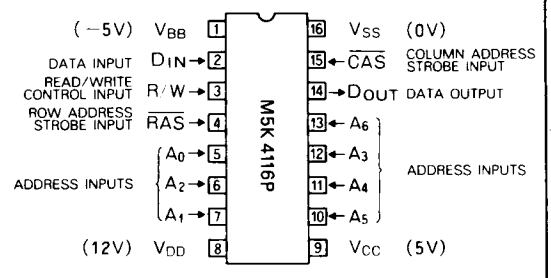
M5K 4116 P-2, S-2; P-3, S-3; P-4, S-4

16 384-BIT (16 384-WORD BY 1-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 16 384-word by 1-bit dynamic RAMs, fabricated with the N-channel silicon-gate MOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential. The use of double-layer poly-silicon process technology and a single-transistor dynamic storage cell provide high circuit density at reduced costs, and the use of dynamic circuitry including sense amplifiers assures low power dissipation. Multiplexed address inputs permit both a reduction in pins to the standard 16-pin package configuration and an increase in system densities.

PIN CONFIGURATION (TOP VIEW)



Outline 16P1 (M5K4116P)
16S1 (M5K4116S)

FEATURES

Type name	Access time (max) (ns)	Cycle time (min) (ns)	Power dissipation (typ) (mW)
M5K 4116P-2, S-2	150	320	330
M5K 4116P-3, S-3	200	375	280
M5K 4116P-4, S-4	250	410	260

- Standard 16-pin package
- Voltage range on all power supplies (V_{DD}, V_{CC}, V_{BB}): ±10%
- Low standby power dissipation: 19.8mW (max)
- Low operating power dissipation: 462mW (max)
- Unlatched output enables two-dimensional chip selection and extended page boundary
- Early-write operation gives common I/O capability
- Read-modify-write, $\overline{RAS}$-only refresh, and page-mode capabilities
- All input terminals have low input capacitance and are directly TTL-compatible
- Output is three-state and directly TTL-compatible
- 128 refresh cycles
- Interchangeable with Mostek's MK4116 in both electrical characteristics and pin configuration

APPLICATION

- Main memory unit for computers

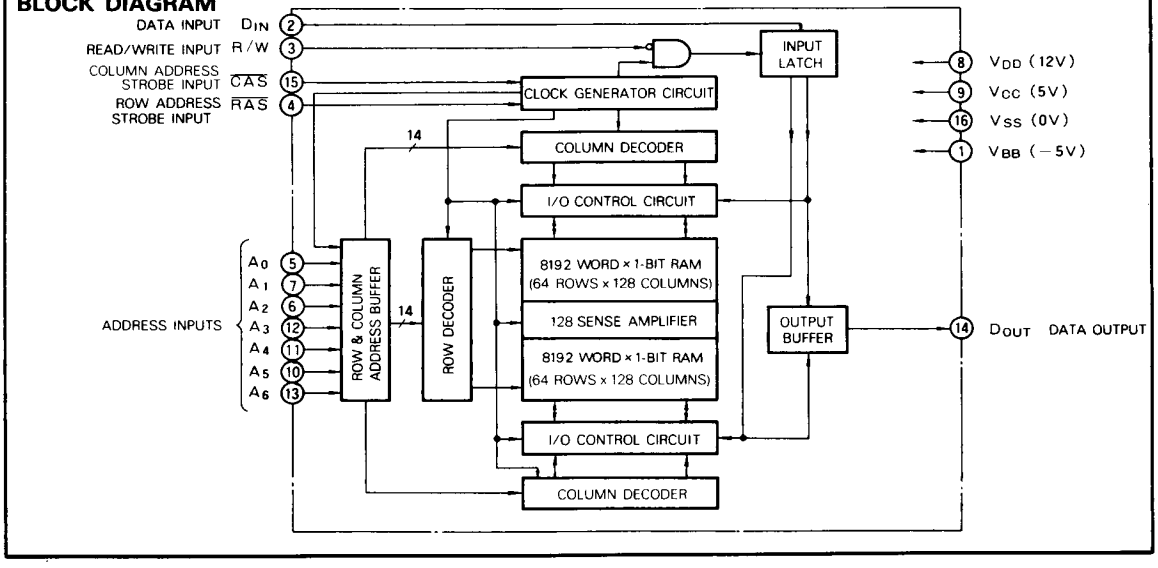
FUNCTION

The M5K4116P and S provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown below.

Operation	Inputs						Output	Re-fresh	Remarks
	$\overline{RAS}$	$\overline{CAS}$	R/W	D_{IN}	Row address	Column address	D_{OUT}		
Read	ACT	ACT	NAC	DNC	APD	APD	VLD	YES	Page mode identical except refresh is NO
Write	ACT	ACT	ACT	VLD	APD	APD	OPN	YES	
Read-modify-write	ACT	ACT	ACT	VLD	APD	APD	VLD	YES	
$\overline{RAS}$-only refresh	ACT	NAC	DNC	DNC	APD	DNC	OPN	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note : ACT : active ; NAC : nonactive ; DNC : don't care ; VLD : valid ; APD : applied ; OPN : open

BLOCK DIAGRAM



16 384-BIT (16 384-WORD BY 1-BIT) DYNAMIC RAM

SUMMARY OF OPERATIONS

Addressing

To select one of the 16 384 memory cells in the M5K 4116 P and S, the 14-bit address signal must be multiplexed into 7 address signals, which are then latched into the on-chip latch by two externally-applied clock pulses. First, the negative-going edge of the row-address-strobe pulse ($\overline{RAS}$) latches the 7 row-address bits; next, the negative-going edge of the column-address-strobe pulse ($\overline{CAS}$) latches the 7 column-address bits. Timing of the $\overline{RAS}$ and $\overline{CAS}$ clocks can be selected by either of the following two methods:

1. The delay time from $\overline{RAS}$ to $\overline{CAS}$ $t_{d(\overline{RAS}\text{-}\overline{CAS})}$ is set between the minimum and maximum values of the limits. In this case, the internal $\overline{CAS}$ control signals are inhibited almost until $t_{d(\overline{RAS}\text{-}\overline{CAS})max}$ ('gated $\overline{CAS}$' operation). The external $\overline{CAS}$ signal can be applied with a margin not affecting the on-chip circuit operations, e.g. access time, and the address inputs can be easily changed from row address to column address.
2. The delay time $t_{d(\overline{RAS}\text{-}\overline{CAS})}$ is set larger than the maximum value of the limits. In this case the internal inhibition of $\overline{CAS}$ has already been released, so that the internal $\overline{CAS}$ control signals are controlled by the externally applied $\overline{CAS}$, which also controls the access time.

Data Input

Data to be written into a selected cell is strobed by the later of the two negative transitions of R/W input and $\overline{CAS}$ input. Thus when the R/W input makes its negative transition prior to $\overline{CAS}$ input (early write), the data input is strobed by $\overline{CAS}$, and the negative transition of $\overline{CAS}$ is set as the reference point for set-up and hold times. In the read-write or read-modify-write cycles, however, when the R/W input makes its negative transition after $\overline{CAS}$, the R/W negative transition is set as the reference point for set-up and hold times.

Data Output Control

The output of the M5K 4116 P and S is in the high-impedance state when $\overline{CAS}$ is high. When the memory cycle in progress is a read, read-modify-write, or a delayed-write cycle, the data output will go from the high-impedance state to the active condition, and the data in the selected cell will be read. This data output will have the same polarity as the input data. Once the output has entered the active condition, this condition will be maintained until $\overline{CAS}$ goes high, irrespective of the condition of $\overline{RAS}$ (for a maximum of 10μs).

The output will remain in the high-impedance state throughout the entire cycle in an early-write cycle.

These output conditions, of the M5K 4116 P and S, which can readily be changed by controlling the timing of the write pulse in a write cycle, and the width of the $\overline{CAS}$ pulse in a read cycle, offer capabilities for a number of applications, as follows.

1. Common I/O Operation

If all write operations are performed in the early-write mode, input and output can be connected directly to give a common I/O data bus.

2. Data Output Hold

The data output can be held between read cycles, without lengthening the cycle time, until the next cycle commences. This enables extremely flexible clock-timing settings for $\overline{RAS}$ and $\overline{CAS}$.

3. Two Methods of Chip Selection

Since the output is not latched, $\overline{CAS}$ is not required to keep the outputs of selected chips in the matrix in a high-impedance state. This means that $\overline{CAS}$ and/or $\overline{RAS}$ can both be decoded for chip selection.

4. Extended-Page Boundary

By decoding $\overline{CAS}$, the page boundary can be extended beyond the 128 column locations in a single chip. In this case, $\overline{RAS}$ must be applied to all devices.

Page-Mode Operation

This operation allows for multiple-column addressing at the same row address, and eliminates the power dissipation associated with the negative-going edge of $\overline{RAS}$, because once the row address has been strobed, $\overline{RAS}$ is maintained. Also, the time required to strobe in the row address for the second and subsequent cycles is eliminated, thereby decreasing the access and cycle times.

Refresh

The refreshing of the dynamic cell matrix is accomplished by performing a memory operation at each of the 128 row-address locations within a 2ms time interval. Any normal memory cycle will perform the refreshing, and $\overline{RAS}$-only refresh offers a significant reduction in operating power.

Power Dissipation

Most of the circuitry in the M5K 4116 P and S is dynamic, and most of the power is dissipated when addresses are strobed. Both $\overline{RAS}$ and $\overline{CAS}$ are decoded and applied to the M5K 4116 P and S as chip-select in the memory system, but if RAS is decoded, all unselected devices go into stand-by independent of the $\overline{CAS}$ condition, minimizing system power dissipation.

Power Supplies

Although the M5K 4116 P and S require no particular power-supply sequencing so long as the devices are used within the limits of the absolute maximum ratings, it is recommended that the V_{BB} supply be applied first and removed last. V_{BB} should never be more positive than V_{SS} when power supply is applied to V_{DD}.

Some eight dummy cycles are necessary after power is applied to the device before memory operation is achieved.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Conditions	Limits	Unit
V_{DD}	Supply voltage		With respect to V_{BB}	−0.5 ~ 20	V
V_{CC}	Supply voltage			−0.5 ~ 20	V
V_{SS}	Supply voltage			−0.5 ~ 20	V
V_I	Input voltage			−0.5 ~ 20	V
V_O	Output voltage			−0.5 ~ 20	V
V_{DD}	Supply voltage		With respect to V_{SS}	−1 ~ 15	V
V_{CC}	Supply voltage			−1 ~ 15	V
$V_{BB}-V_{SS}$	Supply voltage		$V_{DD}-V_{SS}>0$	0	V
I_O	Output current			50	mA
P_d	Power dissipation	M5K4116S	Ta = 25℃	1000	mW
		M5K4116P	Ta = 25℃	700	mW
T_{opr}	Operating free-air temperature range			0 ~ 70	℃
T_{stg}	Storage temperature range	M5K4116S		−65 ~ 150	℃
		M5K4116P		−40 ~ 125	℃

RECOMMENDED OPERATING CONDITIONS (Ta = 0 ~ 70℃, unless otherwise noted. Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{DD}	Supply voltage	10.8	12	13.2	V
V_{CC}	Supply voltage (Note 2)	4.5	5	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{BB}	Supply voltage	−4.5	−5	−5.7	V
V_{IH1}	High-level input voltage, $\overline{RAS}$, $\overline{CAS}$, R/$\overline{W}$	2.7		7	V
V_{IH2}	High-level input voltage, $A_0 \sim A_6$, D_{IN}	2.4		7	V
V_{IL}	Low-level input voltage, all inputs	−1		0.8	V

Note 1 : All voltages with respect to V_{SS}. Apply V_{BB} power supply first, prior to other power supplies, and remove last.

2 : The output voltage will swing from V_{SS} to V_{CC} when output loading current is zero. In standby mode V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention, but the V_{OH} min specification is not guaranteed in this mode.

ELECTRICAL CHARACTERISTICS

(Ta = 0 ~ 70℃, V_{DD} = 12V ± 10%, V_{CC} = 5V ± 10%, V_{SS} = 0V, $-5.7V \leq V_{BB} \leq -4.5V$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{OH}	High-level output voltage (Note 2)	I_{OH} = −5mA	2.4		V_{CC}	V
V_{OL}	Low-level output voltage (Note 2)	I_{OL} = 4.2mA	0		0.4	V
I_{OZ}	Off-state output current	D_{OUT} floating $0V \leq V_{OUT} \leq 5.5V$	−10		10	μA
I_I	Input current	V_{BB} = −5V, $0V \leq V_{IN} \leq 7V$ All other pins = 0V	−10		10	μA
$I_{DD1(AV)}$	Average supply current from V_{DD}, operating	$\overline{RAS}$, $\overline{CAS}$ cycling $t_{c(RD)} = t_{c(WR)}$ = min			35	mA
$I_{CC1(AV)}$	Average supply current from V_{CC}, operating (Note 4)				—	—
$I_{BB1(AV)}$	Average supply current from V_{BB}, operating				200	μA
I_{DD2}	Supply current from V_{DD}, standby	$\overline{RAS}$ = V_{IH} D_{OUT} = floating			1.5	mA
I_{CC2}	Supply current from V_{CC}, standby		−10		10	μA
I_{BB2}	Supply current from V_{BB}, standby				100	μA
$I_{DD3(AV)}$	Average supply current from V_{DD}, refreshing	$\overline{RAS}$ cycling $\overline{CAS}$ = V_{IH} $t_{c(REF)}$ = min			27	mA
$I_{CC3(AV)}$	Average supply current from V_{CC}, refreshing		−10		10	μA
$I_{BB3(AV)}$	Average supply current from V_{BB}, refreshing				200	μA
$I_{DD4(AV)}$	Average supply current from V_{DD}, page mode	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling $t_{c(PG)}$ = min			27	mA
$I_{CC4(AV)}$	Average supply current from V_{CC}, page mode (Note 4)				—	—
$I_{BB4(AV)}$	Average supply current from V_{BB}, page mode				200	μA
$C_{i(AD)}$	Input capacitance, address inputs	V_I = V_{SS} f = 1MHz V_I = 25mVrms			5	pF
$C_{i(DA)}$	Input capacitance, data input				5	pF
$C_{i(R/W)}$	Input capacitance, read/write control input				7	pF
$C_{i(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input				10	pF
$C_{i(\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input				10	pF
C_O	Output capacitance	V_O = V_{SS}, f = 1MHz, V_I = 25mVrms			7	pF

Note 3 Except for I_{BB}, current flowing into an IC is positive ; out is negative.

4 : V_{CC} is connected only to the output buffer, so that I_{CC1} and I_{CC4} depend upon output loading.

16 384-BIT (16 384-WORD BY 1-BIT) DYNAMIC RAM

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Page-Mode Cycles)

($Ta = 0 \sim 70℃$, $V_{DD} = 12V \pm 10\%$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, $-5.7V \leq V_{BB} \leq -4.5V$, unless otherwise noted. See notes 5, 6, and 7.)

Symbol	Parameter	Alternative Symbol	M5K 4116 P-2, S-2 Limits		M5K 4116 P-3, S-3 Limits		M5K 4116 P-4, S-4 Limits		Unit
			Min	Max	Min	Max	Min	Max	
$t_{C(\overline{REF})}$	Refresh cycle time	t_{REF}		2		2		2	ms
$t_{W(\overline{RASH})}$	$\overline{RAS}$ high pulse width	t_{RP}	100		120		150		ns
$t_{W(\overline{RASL})}$	$\overline{RAS}$ low pulse width	t_{RAS}	150	10000	200	10000	250	10000	ns
$t_{W(\overline{CASL})}$	$\overline{CAS}$ low pulse width (Note 8)	t_{CAS}	100		135		165		ns
$t_{h(\overline{RAS}\text{-}\overline{CAS})}$	$\overline{CAS}$ hold time with respect to $\overline{RAS}$	t_{CSH}	150		200		250		ns
$t_{h(\overline{CAS}\text{-}\overline{RAS})}$	$\overline{RAS}$ hold time with respect to $\overline{CAS}$	t_{RSH}	100		135		165		ns
$t_{d(\overline{RAS}\text{-}\overline{CAS})}$	Delay time, $\overline{RAS}$ to $\overline{CAS}$ (Note 9)	t_{RCD}	20	50	25	65	35	85	ns
$t_{d(\overline{CAS}\text{-}\overline{RAS})}$	Delay time, $\overline{CAS}$ to $\overline{RAS}$	t_{CRP}	−20		−20		−20		ns
$t_{su(RA\text{-}\overline{RAS})}$	Row address setup time with respect to $\overline{RAS}$	t_{ASR}	0		0		0		ns
$t_{su(CA\text{-}\overline{CAS})}$	Column address setup time with respect to $\overline{CAS}$	t_{ASC}	−10		−10		−10		ns
$t_{h(\overline{RAS}\text{-}RA)}$	Row address hold time with respect to $\overline{RAS}$	t_{RAH}	20		25		35		ns
$t_{h(\overline{CAS}\text{-}CA)}$	Column address hold time with respect to $\overline{CAS}$	t_{CAH}	45		55		75		ns
$t_{h(\overline{RAS}\text{-}CA)}$	Column address hold time with respect to $\overline{RAS}$	t_{AR}	95		120		160		ns
t_{THL} t_{TLH}	Transition time	t_T	3	35	3	50	3	50	ns

Note 5 : After power supply is applied, some eight dummy cycles are required before memory operation is achieved. $\overline{RAS}/\overline{CAS}$ refresh cycles or $\overline{RAS}$ read-only cycles are suitable as dummy cycles. Once power is applied, it is also recommended to keep the $\overline{RAS}$ at high-level for more than 3μs before the dummy cycles, or to keep the $\overline{RAS}$ high pulse width $t_{W(\overline{RASH})}$ more than 3μs for a minimum of one dummy cycle.

6 : The switching characteristics are defined as $t_{THL} = t_{TLH} = 5ns$.

7 : Reference levels of input signals are V_{IH1} min, V_{IH2} min and V_{IL} max. Reference levels for transition time are also between V_{IH1} or V_{IH2} and V_{IL}.

8 : Assumes that $t_{d(\overline{RAS}\text{-}\overline{CAS})} \geq t_{d(\overline{RAS}\text{-}\overline{CAS})}$ max. If $t_{d(\overline{RAS}\text{-}\overline{CAS})} < t_{d(\overline{RAS}\text{-}\overline{CAS})}$ max., $t_{W(\overline{CASL})}$ will be increased by the amount that $t_{d(\overline{RAS}\text{-}\overline{CAS})}$ has decreased.

9 : The maximum value of $t_{d(\overline{RAS}\text{-}\overline{CAS})}$ does not define the limit of operation, but is specified as a reference point only; if $t_{d(\overline{RAS}\text{-}\overline{CAS})}$ is greater than the specified $t_{d(\overline{RAS}\text{-}\overline{CAS})}$ max limit, then access time is controlled exclusively by $t_{a(\overline{CAS})}$.

SWITCHING CHARACTERISTICS ($Ta = 0 \sim 70℃$, $V_{DD} = 12V \pm 10\%$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, $-5.7V \leq V_{BB} \leq -4.5V$, unless otherwise noted)

Read Cycle

Symbol	Parameter	Alternative Symbol	M5K 4116 P-2, S-2 Limits		M5K 4116 P-3, S-3 Limits		M5K 4116 P-4, S-4 Limits		Unit
			Min	Max	Min	Max	Min	Max	
$t_{C(RD)}$	Read cycle time	t_{RC}	320		375		410		ns
$t_{su(RD\text{-}\overline{CAS})}$	Read set-up time with respect to $\overline{CAS}$	t_{RCS}	0		0		0		ns
$t_{h(\overline{CAS}\text{-}RD)}$	Read hold time with respect to $\overline{CAS}$	t_{RCH}	0		0		0		ns
$t_{h(\overline{CAS}\text{-}OUT)}$	Data-out hold time	t_{OFF}	0	40	0	50	0	60	ns
$t_{a(\overline{CAS})}$	$\overline{CAS}$ access time (Note 10)	t_{CAC}		100		135		165	ns
$t_{a(\overline{RAS})}$	$\overline{RAS}$ access time (Note 11)	t_{RAC}		150		200		250	ns

Note 10 : This is the value when $t_{d(\overline{RAS}\text{-}\overline{CAS})} \geq t_{d(\overline{RAS}\text{-}\overline{CAS})}$max. Test conditions : Load = 2TTL, $C_L = 100pF$

11 : This is the value when $t_{d(\overline{RAS}\text{-}\overline{CAS})} < t_{d(\overline{RAS}\text{-}\overline{CAS})}$max. When $t_{d(\overline{RAS}\text{-}\overline{CAS})} \geq t_{d(\overline{RAS}\text{-}\overline{CAS})}$max., $t_{a(\overline{RAS})}$ increases by the amount of increase of $t_{d(\overline{RAS}\text{-}\overline{CAS})}$. Test conditions : Load = 2TTL, $C_L = 100pF$

Write Cycle

Symbol	Parameter	Alternative Symbol	M5K 4116 P-2, S-2 Limits		M5K 4116 P-3, S-3 Limits		M5K 4116 P-4, S-4 Limits		Unit
			Min	Max	Min	Max	Min	Max	
$t_{C(WR)}$	Write cycle time	t_{RC}	320		375		410		ns
$t_{su(WR\text{-}\overline{CAS})}$	Write set-up time with respect to $\overline{CAS}$ (Note 12)	t_{WCS}	−20		−20		−20		ns
$t_{h(\overline{CAS}\text{-}WR)}$	Write hold time with respect to $\overline{CAS}$	t_{WCH}	45		55		75		ns
$t_{h(\overline{RAS}\text{-}WR)}$	Write hold time with respect to $\overline{RAS}$	t_{WCR}	95		120		160		ns
$t_{h(WR\text{-}\overline{RAS})}$	$\overline{RAS}$ hold time with respect to write	t_{RWL}	50		70		85		ns
$t_{h(WR\text{-}\overline{CAS})}$	$\overline{CAS}$ hold time with respect to write	t_{CWL}	50		70		85		ns
$t_{W(WR)}$	Write pulse width	t_{WP}	45		55		75		ns
$t_{su(DA\text{-}\overline{CAS})}$	Data-in setup time with respect to $\overline{CAS}$	t_{DS}	0		0		0		ns
$t_{h(\overline{CAS}\text{-}DA)}$	Data-in hold time with respect to $\overline{CAS}$	t_{DH}	45		55		75		ns
$t_{h(\overline{RAS}\text{-}DA)}$	Data-in hold time with respect to $\overline{RAS}$	t_{DHR}	95		120		160		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Alternative symbol	M5K 4116 P-2, S-2 Limits		M5K 4116 P-3, S-3 Limits		M5K 4116 P-4, S-4 Limits		Unit
			Min	Max	Min	Max	Min	Max	
$t_{C(RMW)}$	Read-modify-write cycle time	t_{RWC}	320		405		500		ns
$t_{C(RW)}$	Read-write cycle time	t_{RWC}	320		375		425		ns
$t_{h(WR-\overline{RAS})}$	$\overline{RAS}$ hold time with respect to write	t_{RWL}	50		70		85		ns
$t_{h(WR-\overline{CAS})}$	$\overline{CAS}$ hold time with respect to write	t_{CWL}	50		70		85		ns
$t_{W(WR)}$	Write pulse width	t_{WP}	45		55		75		ns
$t_{su(RD-\overline{CAS})}$	Read setup time with respect to $\overline{CAS}$	t_{RCS}	0		0		0		ns
$t_{d(\overline{RAS}-WR)}$	Delay time, $\overline{RAS}$ to write (Note 12)	t_{RWD}	110		145		175		ns
$t_{d(\overline{CAS}-WR)}$	Delay time, $\overline{CAS}$ to write (Note 12)	t_{CWD}	60		80		90		ns
$t_{su(DA-WR)}$	Data-in set-up time with respect to write	t_{DS}	0		0		0		ns
$t_{h(WR-DA)}$	Data-in hold time with respect to write	t_{DH}	45		55		75		ns
$t_{h(\overline{CAS}-OUT)}$	Data-out hold time with respect to $\overline{CAS}$	t_{OFF}	0	40	0	50	0	60	ns
$t_{a(\overline{CAS})}$	$\overline{CAS}$ access time (Note 10)	t_{CAC}		100		135		165	ns
$t_{a(\overline{RAS})}$	$\overline{RAS}$ access time (Note 11)	t_{RAC}		150		200		250	ns

Note 12 : $t_{su(WR-\overline{CAS})}$, $t_{d(\overline{RAS}-WR)}$, and $t_{d(\overline{CAS}-WR)}$ do not define the limits of operation, but are included as electrical characteristics only.
When $t_{su(WR-\overline{CAS})} \geqq t_{su(WR-\overline{CAS})min}$, an early-write cycle is performed, and the data output keeps the high-impedance state.
When $t_{d(\overline{RAS}-WR)} \geqq t_{d(\overline{RAS}-WR)min}$ and $t_{d(\overline{CAS}-WR)} \geqq t_{d(\overline{CAS}-WR)min}$, a read-modify-write cycle is performed, and the data of the selected address will be read out on the data outputs.
For all conditions other than those described above the condition of data output is not defined.

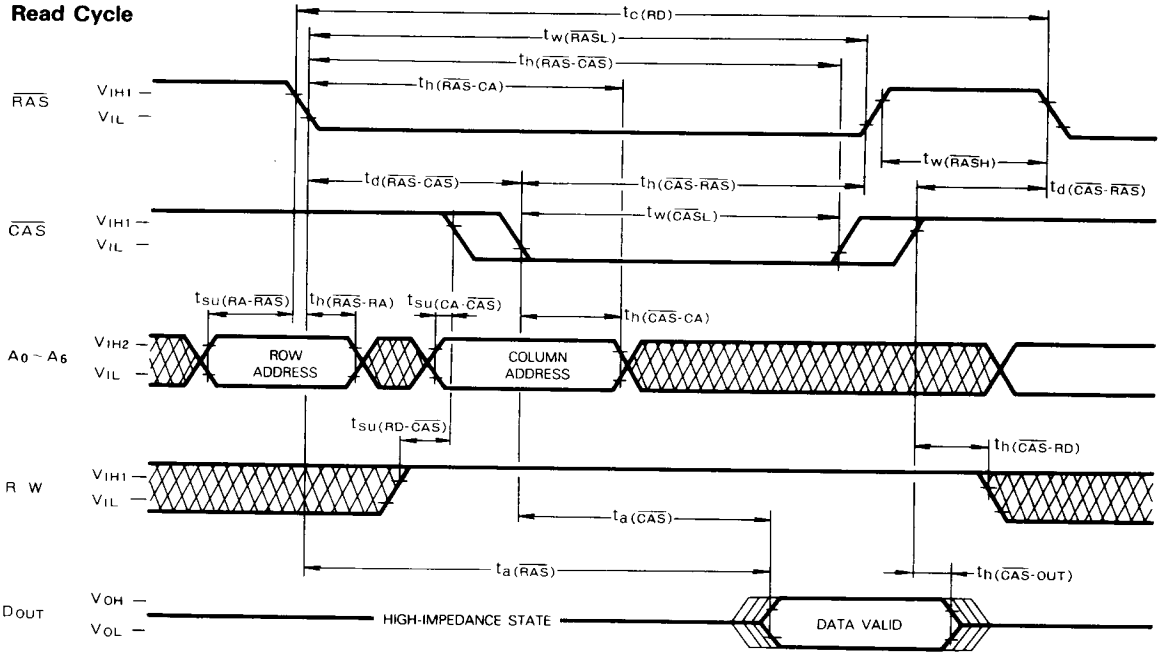
Page-Mode Cycle

Symbol	Parameter	Alternative symbol	M5K 4116 P-2, S-2 Limits		M5K 4116 P-3, S-3 Limits		M5K 4116 P-4, S-4 Limits		Unit
			Min	Max	Min	Max	Min	Max	
$t_{C(PG)}$	Page-mode cycle time	t_{PC}	170		225		275		ns
$t_{W(\overline{CAS}H)}$	$\overline{CAS}$ high pulse width	t_{CP}	60		80		100		ns

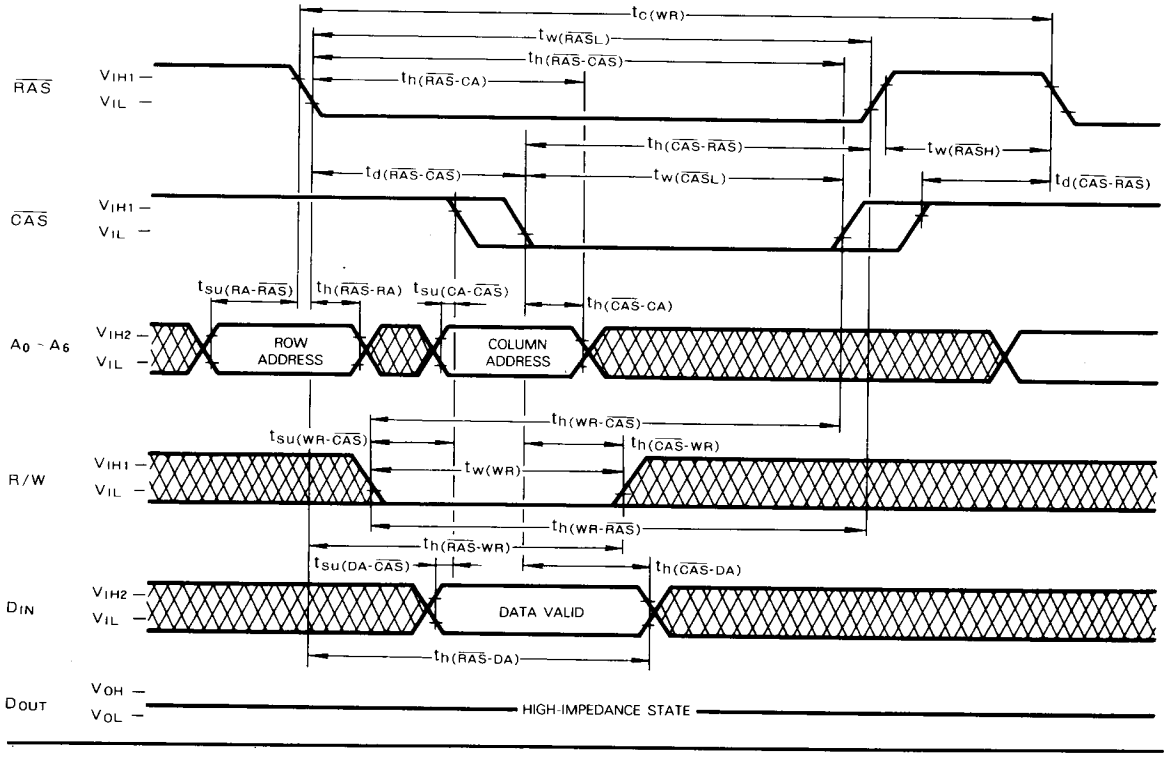
16 384-BIT (16 384-WORD BY 1-BIT) DYNAMIC RAM

TIMING DIAGRAMS

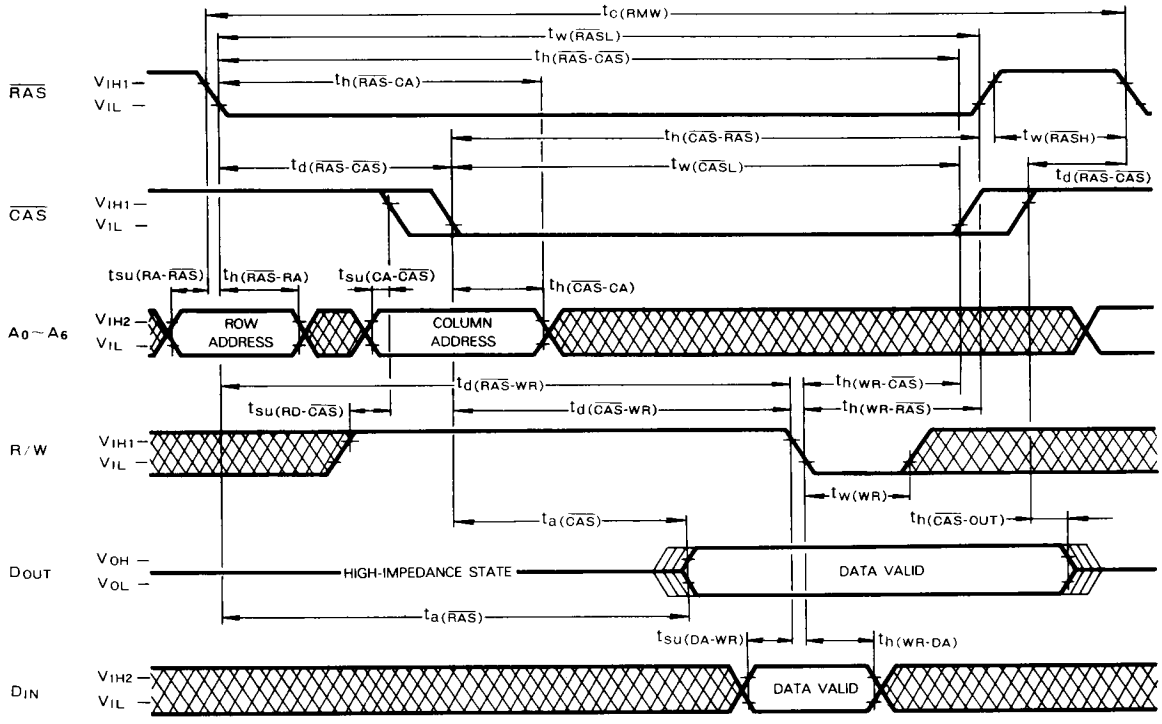
Read Cycle



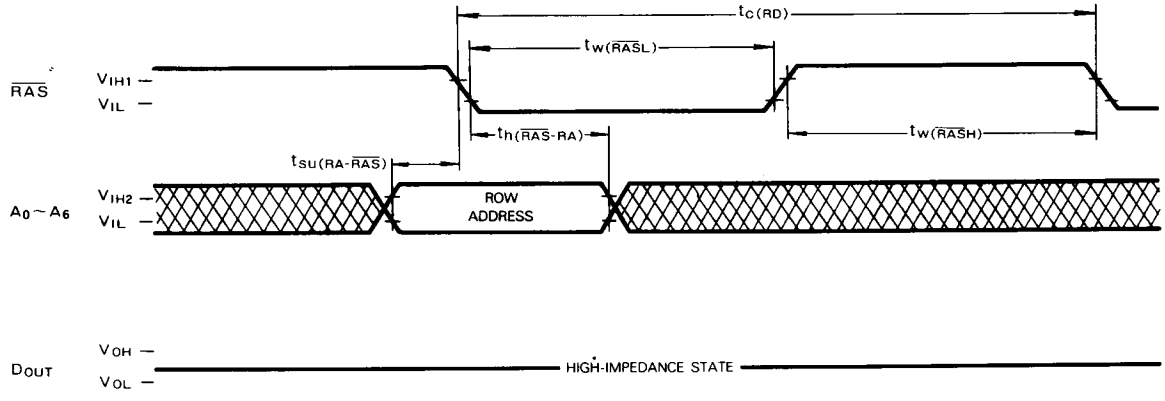
Write and Early Write Cycles



Read-Write and Read-Modify-Write Cycles



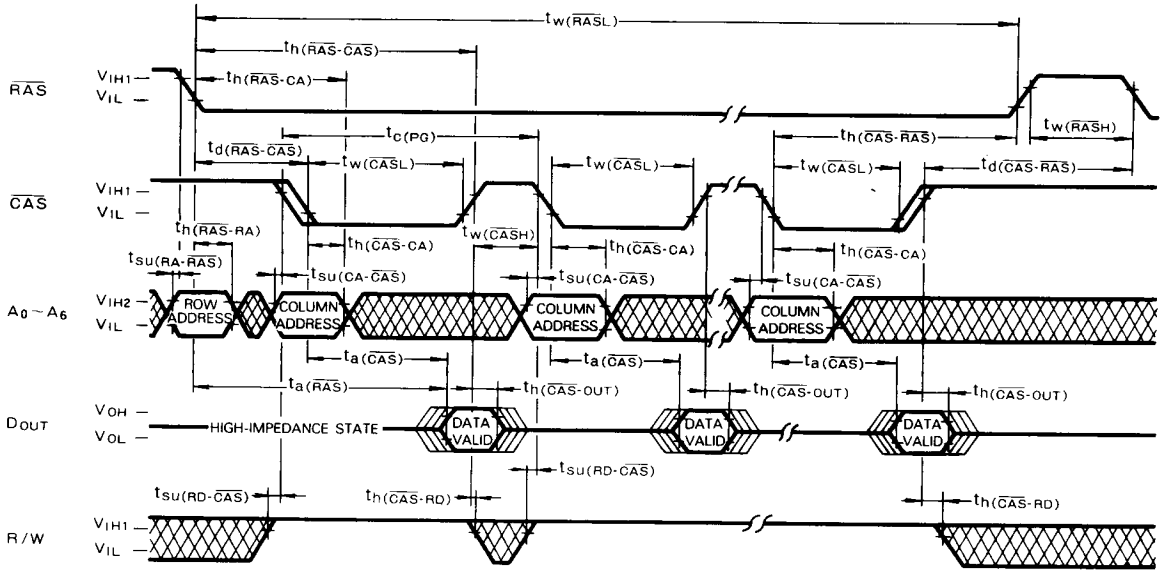
RAS-Only Refresh Cycle



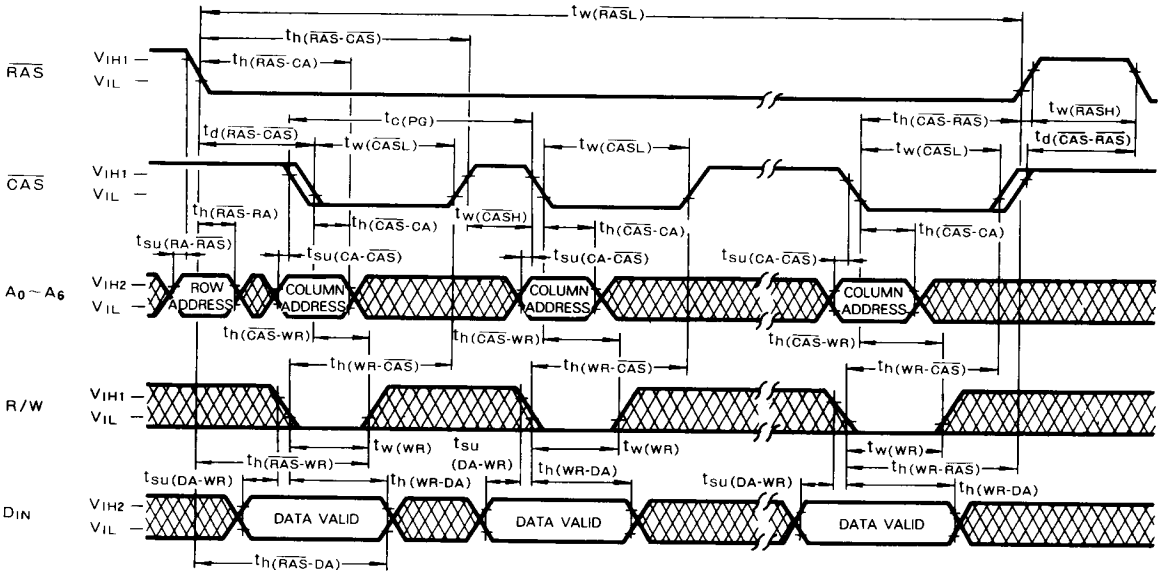
Note 13 : $\overline{CAS}$ = V_{IH1}, R/W = don't care.

16 384-BIT (16 384-WORD BY 1-BIT) DYNAMIC RAM

Page-Mode Read Cycle



Page-Mode Write Cycle



Note 14 :

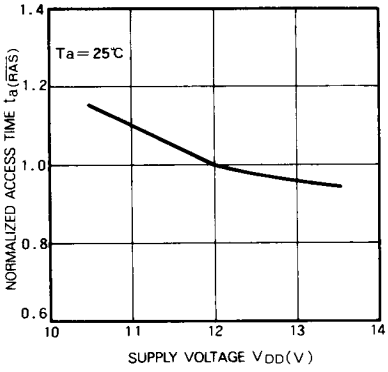
Indicates the don't care input.

The center-line indicates the high-impedance state.

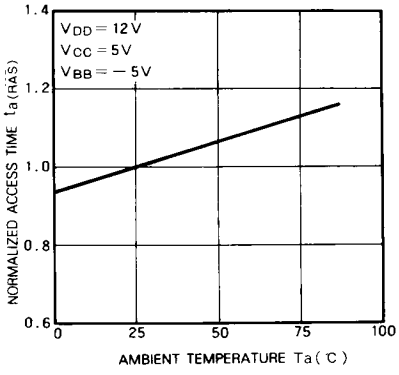
MITSUBISHI ELECTRIC

TYPICAL CHARACTERISTICS

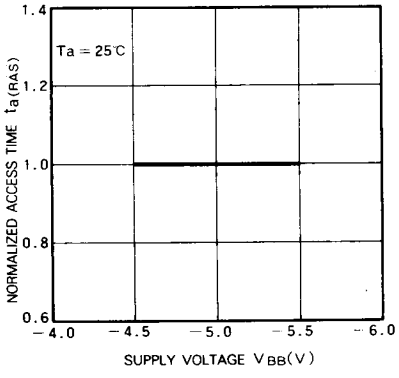
NORMALIZED ACCESS TIME VS. SUPPLY VOLTAGE V_{DD}



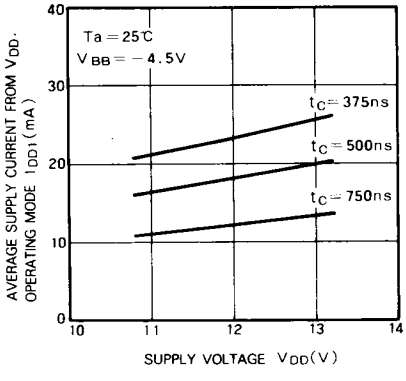
NORMALIZED ACCESS TIME VS. AMBIENT TEMPERATURE



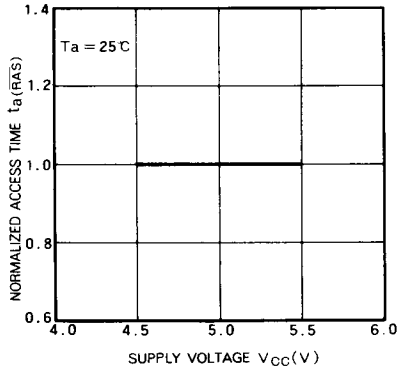
NORMALIZED ACCESS TIME VS. SUPPLY VOLTAGE V_{BB}



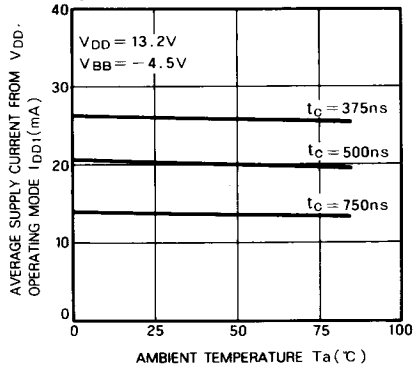
AVERAGE SUPPLY CURRENT FROM V_{DD}, OPERATING MODE VS. SUPPLY VOLTAGE



NORMALIZED ACCESS TIME VS. SUPPLY VOLTAGE V_{CC}

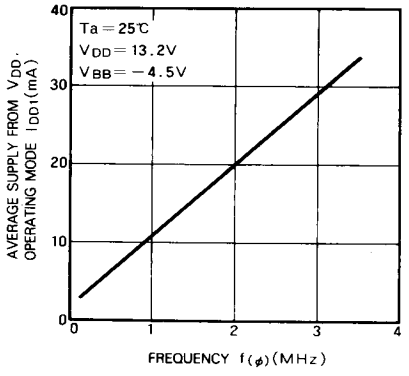


AVERAGE SUPPLY CURRENT FROM V_{DD}, OPERATING MODE VS. AMBIENT TEMPERATURE

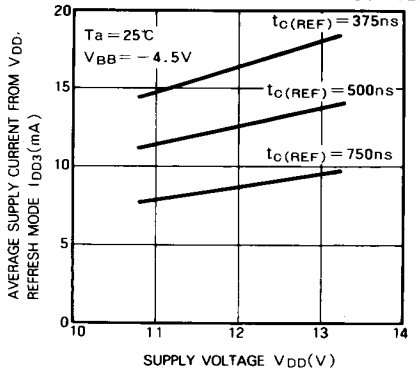


16 384-BIT (16 384-WORD BY 1-BIT) DYNAMIC RAM

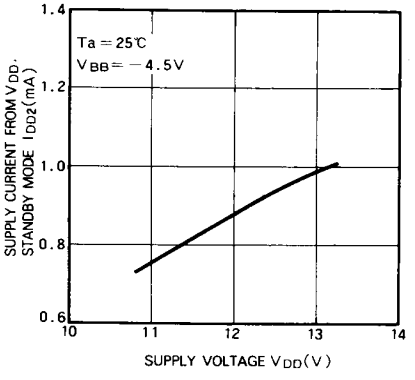
AVERAGE SUPPLY CURRENT FROM V_{DD}, OPERATING MODE VS. FREQUENCY



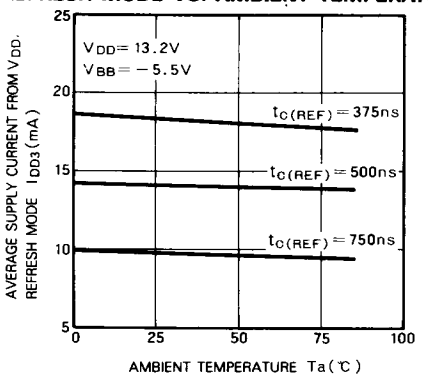
AVERAGE SUPPLY CURRENT FROM V_{DD}, REFRESH MODE VS. SUPPLY VOLTAGE



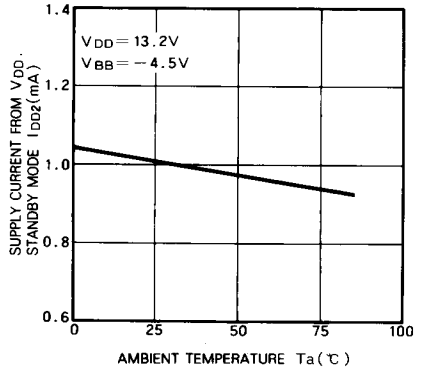
SUPPLY CURRENT FROM V_{DD}, STANDBY MODE VS. SUPPLY VOLTAGE



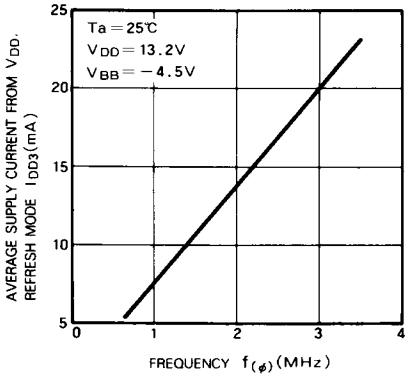
AVERAGE SUPPLY CURRENT FROM V_{DD}, REFRESH MODE VS. AMBIENT TEMPERATURE



SUPPLY CURRENT FROM V_{DD}, STANDBY MODE VS. AMBIENT TEMPERATURE

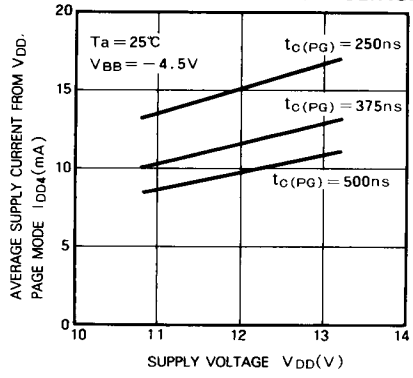


AVERAGE SUPPLY CURRENT FROM V_{DD}, REFRESH MODE VS. FREQUENCY

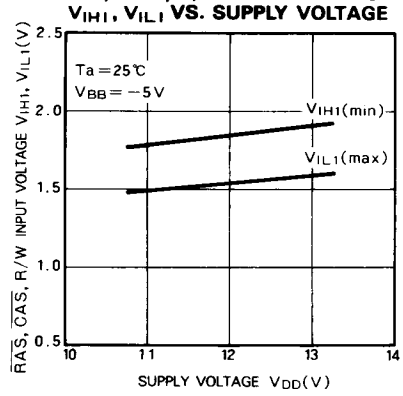


MITSUBISHI ELECTRIC

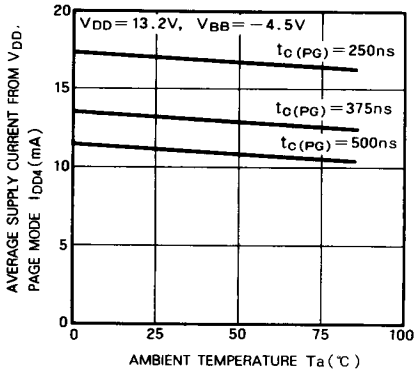
AVERAGE SUPPLY CURRENT FROM V_{DD}, PAGE MODE VS. SUPPLY VOLTAGE



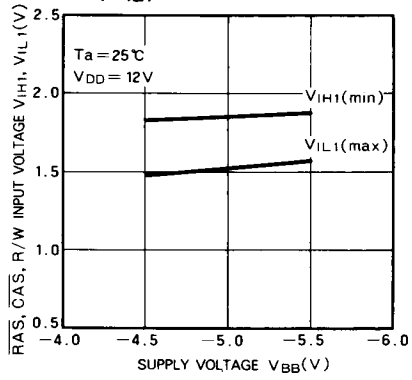
$\overline{RAS}$, $\overline{CAS}$, R/W INPUT VOLTAGE V_{IH1}, V_{IL1} VS. SUPPLY VOLTAGE



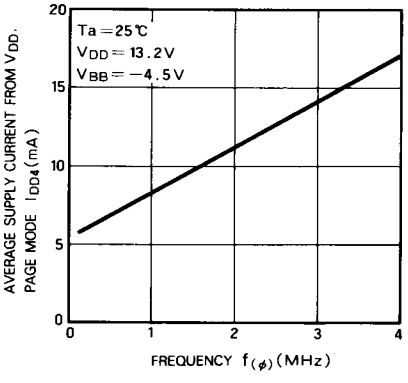
AVERAGE SUPPLY CURRENT FROM V_{DD}, PAGE MODE VS. AMBIENT TEMPERATURE



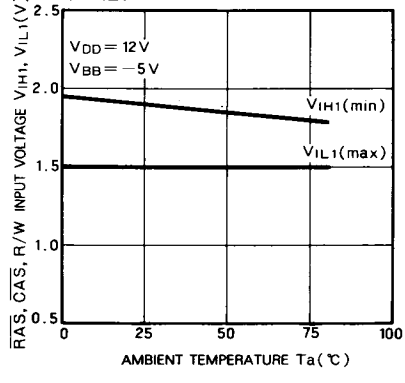
$\overline{RAS}$, $\overline{CAS}$, R/W INPUT VOLTAGE V_{IH1}, V_{IL1} VS. SUPPLY VOLTAGE



AVERAGE SUPPLY CURRENT FROM V_{DD}, PAGE MODE VS. FREQUENCY

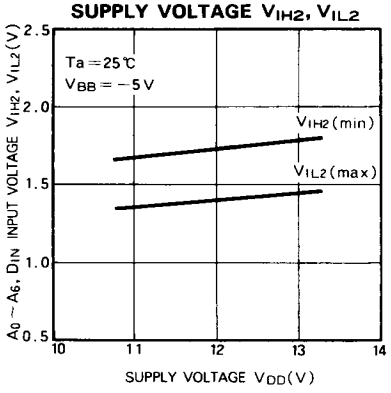


$\overline{RAS}$, $\overline{CAS}$, R/W INPUT VOLTAGE V_{IH1}, V_{IL1} VS. AMBIENT TEMPERATURE

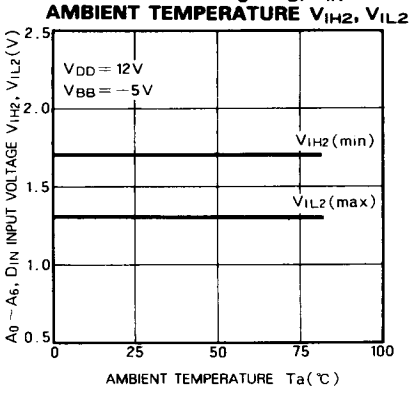


16 384-BIT (16 384-WORD BY 1-BIT) DYNAMIC RAM

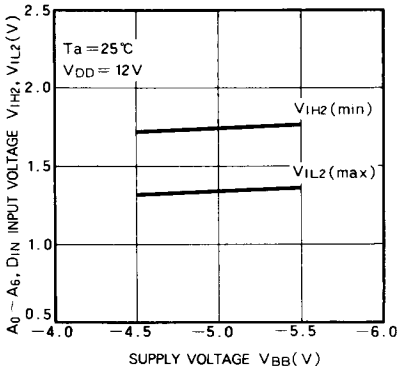
INPUT VOLTAGE $A_0 \sim A_6$, D_{IN} VS. SUPPLY VOLTAGE V_{IH2}, V_{IL2}



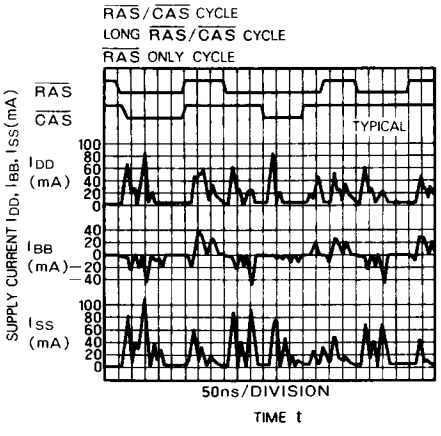
INPUT VOLTAGE $A_0 \sim A_6$, D_{IN} VS. AMBIENT TEMPERATURE V_{IH2}, V_{IL2}



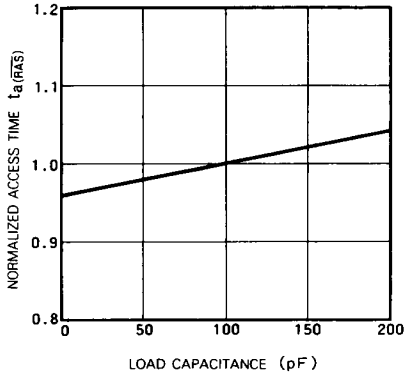
INPUT VOLTAGE $A_0 \sim A_6$, D_{IN} VS. SUPPLY VOLTAGE V_{IH2}, V_{IL2}



SUPPLY CURRENT VS. TIME



NORMALIZED ACCESS TIME VS. LOAD CAPACITANCE



MITSUBISHI ELECTRIC