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Enhanced Memory Expansion Adapter

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Enhanced Memory Expansion Adapter

Third Edition (July 1987)

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Notes:

Preface

This manual describes the three major portions of the Enhanced Memory Expansion Adapter: memory, the serial port, and the parallel port. It also has information about the switch settings that affect memory as well as the jumpers that affect the serial and parallel ports.

The information in this publication is for reference and is intended for hardware and program designers, system programmers, engineers, and anyone else who needs to understand the design and operation of the Adapter.

This manual consists of six sections. Section 1 describes the memory on the adapter. Section 2 describes the switch settings on the adapter. Section 3 and Section 4 describe the serial and parallel portions of the adapter respectively. Section 5 contains hardware specifications, and Section 6 contains logic diagrams.

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Section 1. Memory

Contents

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Description

The Enhanced Memory Expansion Adapter with serial and parallel ports is designed to be used in an IBM Personal Computer AT[1] or the IBM Personal Computer XT[2] Model 286. The adapter memory is organized for a 2-byte system with single-byte read and write capability. The memory will also support a split memory configuration described later in this manual.

Memory is packaged in SIP (Single-In-line Packaging) modules. These modules are organized 256K by 9 bits, 512K by 9 bits, or 1024K by 9 bits. Memory modules are installed in pairs as 512KB, 1024KB or 2048KB, increments depending on the module size used. A total of 12 memory modules can be installed to fill an adapter to 3MB (if all 256KB modules are used), 5MB (if a mix of 256K and 512K modules are used), 6MB (if all 512KB modules are used), or 12MB (if all 1024KB modules are used). When mixing 256K and 512K modules the first two pairs must be 256K modules and all additional pairs must be 512KB modules. Cards with 1MB modules cannot contain any 512KB or 256KB modules.

Memory Cycles

MEMR and MEMW commands require a 1-wait-state, 3-clock memory cycle. Data moves as a byte (8 data bits and 1 parity bit) or as a word (16 data bits and 2 parity bits) and is parity-checked on the adapter. A parity error causes an I/O channel check (non-maskable interrupt) to the system.

I/O Channel Check

When the I/O channel check occurs, a non-maskable interrupt (NMI) results, and the status bits determine the source (one status bit is I/O channel check and the other is system-board parity check). Writing to the failing card will clear the status bit.

1 "Personal Computer AT" is a Registered Trademark of the IBM Corp.
2 "Personal Computer XT" is a Registered Trademarks of the IBM Corp.

Memory Addressing

Memory can be added to both the base memory area and the expansion memory area of the IBM Personal Computer AT or XT Model 286.

The base memory area has an address range from 0 to 640KB. The expansion memory area has an address range from 1024KB to 16,256KB.

The memory address from 640KB to 1024KB and 16,256KB to 16,384KB are reserved for system functions.

Split Memory

The adapter can be used to fill base memory up to its 640KB limit. The additional memory above 640KB automatically becomes part of the expansion memory area.

The capability to split memory between the base memory area and the expansion memory area is called split memory addressing.

Contiguous Memory

If base memory is already filled, an adapter can be used to increase the amount of memory in the expansion memory area of the computer.

Memory on the adapter is added at a starting address directly after the expansion memory. Because there cannot be any gap between newly added memory and existing memory, this is called contiguous memory addressing.

ROM Subsystem Address

The ROM subsystem is assigned to the last 1MB address space (Hex FF0000) in expansion memory. These memory locations cannot be addressed by the adapter. Consequently, when performing setup and configuring expansion memory, a value no greater than 15232KB can be entered without receiving memory errors.

Section 2. Switch Settings

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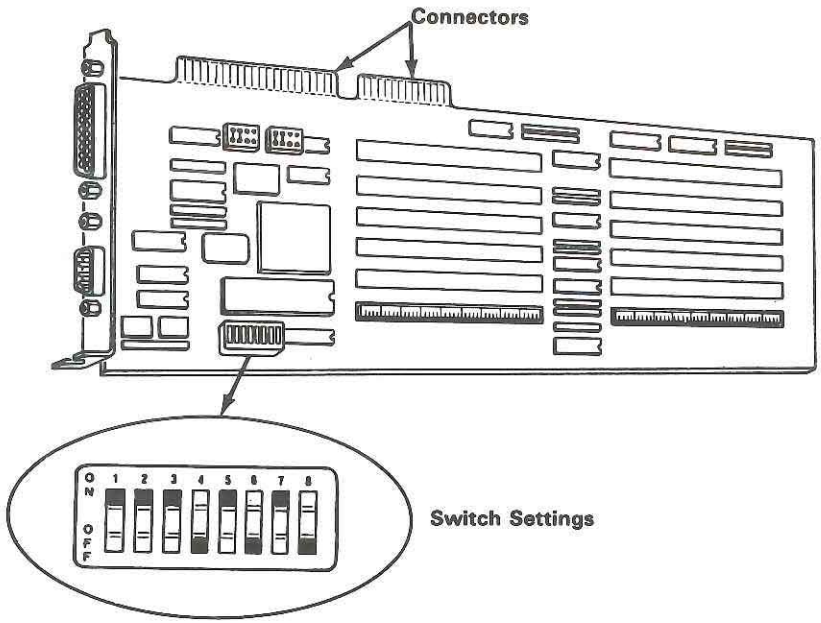
Notes:

Setting the Switches

There are eight rocker switches located together in a block on the adapter. The switches are numbered 1-8. The adapter in the figure is shown with the connectors at the top. This is so the numbers above the switches can be read easily.

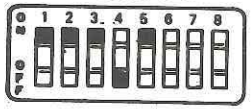
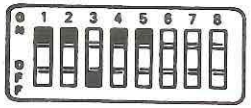
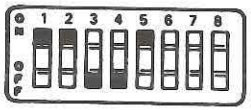
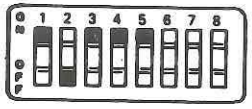
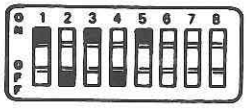
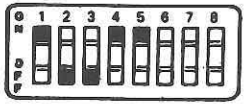
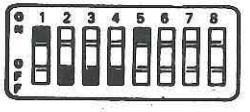
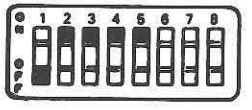


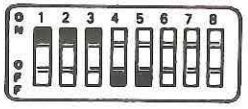
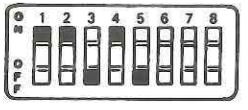
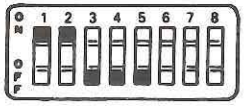
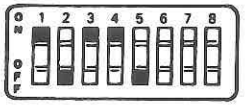
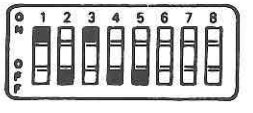
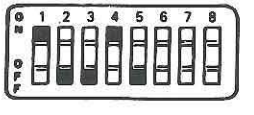
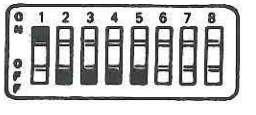
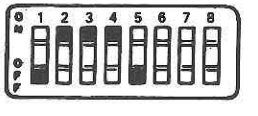
Note: The dark square indicates the end of the switch is depressed.

For example, this switch is set to the ON position.

Switches 1-5

Switches 1-5 determine the starting address of memory added to the expansion memory area. Memory added to this area can have a starting address from 1MB up to 15.5MB.

Starting Address	Switches 1-5
1MB (1024KB)	
2MB (2048KB)	
3MB (3072KB)	
4MB (4096KB)	
5MB (5120KB)	
6MB (6144KB)	
7MB (7168KB)	
8MB (8192KB)	

Starting Address	Switches 1-5
1.5MB (1536KB)	
2.5MB (2560KB)	
3.5MB (3584KB)	
4.5MB (4608KB)	
5.5MB (5632KB)	
6.5MB (6656KB)	
7.5MB (7680KB)	
8.5MB (8704KB)	

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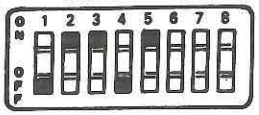
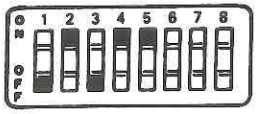
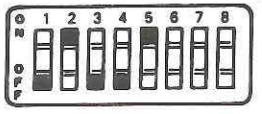
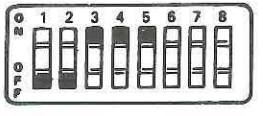
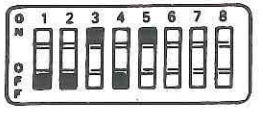
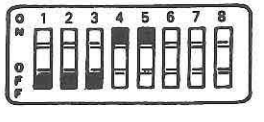
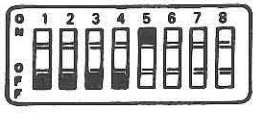
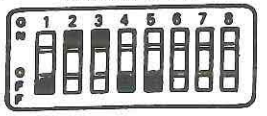
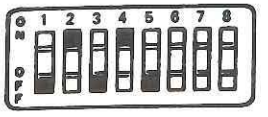
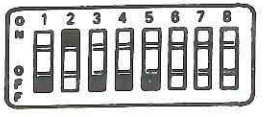
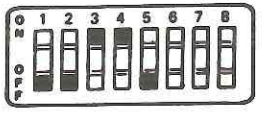
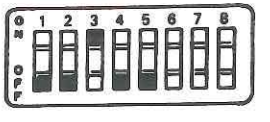
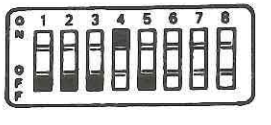
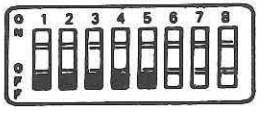
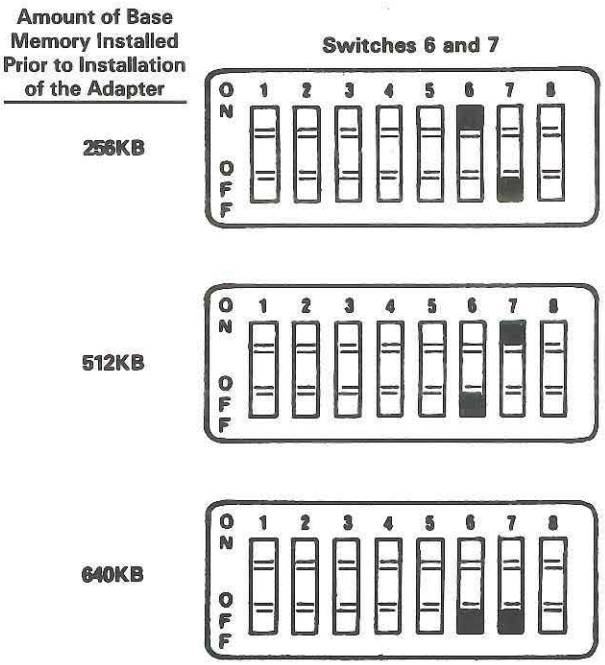
9MB (9216KB)	
10MB (10240KB)	
11MB (11264KB)	
12MB (12288KB)	
13MB (13312KB)	
14MB (14336KB)	
15MB (15360KB)	

Starting Address	Switches 1-5
9.5MB (9728KB)	
10.5MB (10752KB)	
11.5MB (11776KB)	
12.5MB (12800KB)	
13.5MB (13824KB)	
14.5MB (14848KB)	
15.5MB (15872KB)	

Note: It is not necessary to reset the starting address on an adapter when memory modules are added to it. The starting address of memory on the adapter will stay the same. The adapter automatically adjusts for the increase in memory size.

Switches 6 and 7

Switches 6 and 7 determine the starting address of memory that is added to the base memory area. The starting address depends on the amount of base memory currently installed in the computer.



Switch 8

Switch 8 enables or disables the I/O ports on the adapter. In the ON position, the switch enables the ports. In the OFF position, the switch disables the ports.

Switch Definition Summary

The following table summarizes the meaning of each of the 8 switches:

Switch #	Definition
1–5	Starting Address in the Expansion Memory Area
6–7	Starting Address in the Base Memory Area
8	I/O Ports Enable/Disable

Multiple Adapter Cards

You may install up to five Adapters in an IBM Personal Computer AT or up to 4 Adapters in an IBM Personal Computer XT Model 286. The IBM Personal Computer AT or XT Model 286 can use 15.5MB (15872KB) of memory (640KB of base memory and 15232KB of expansion memory).

The switch settings on each adapter will vary depending on the number of adapters and the amount of memory currently installed in the computer.

If a computer contains 640KB of base memory, adapters are added to the expansion memory area. An adapter is configured to start at the first available address in the expansion area. Each remaining adapter is configured to start at the address following the one before it.

If a computer contains 256KB or 512KB of base memory, one adapter can be configured to fill the base memory area. It can be configured to start at a base memory address of 256KB or 512KB, depending on the amount of base memory currently installed. This adapter must have the highest starting address in expansion memory.

Switch number 8 on each adapter is used to enable or disable the I/O ports on that adapter. To enable the I/O ports, switch number 8 should be set ON. To disable the I/O ports, switch number 8 should be set OFF. The IBM Personal Computer AT or XT Model 286 can have at most two serial and two parallel ports enabled. Therefore, a maximum of two adapters can be enabled at the same time.

Note: Three parallel ports can be enabled if one is the parallel port on the monochrome monitor parallel printer adapter.

Section 3. Serial Portion of the Adapter

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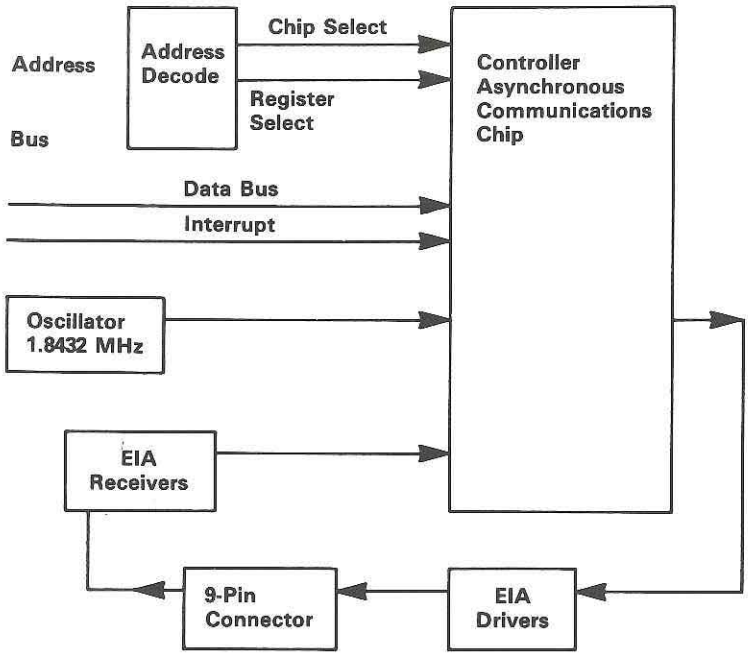
Notes:

Serial Port

The serial portion of the adapter is fully programmable and supports asynchronous communications. It will add and remove start, stop, and parity bits. A programmable baud-rate generator allows operation from 50 baud to 9600 baud. Five-, six-, seven- and eight-bit characters with 1, 1.5, or 2 stop bits are supported. A prioritized interrupt system controls transmit, receive, error, and line status as well as data set interrupts.

The rear of the adapter has a 9-pin D-shell connector that is classified as an RS-232C port. When the optional IBM Communications Cable (9-pin), which has a 9-pin D shell connecter on one end and a 25-pin D-shell connector on the other end, is connected to the adapter, the 25 pin end of the cable has all the signals of a standard EIA RS-232C interface.

The following figure is a block diagram of the serial portion of the adapter.



Serial Portion Block Diagram

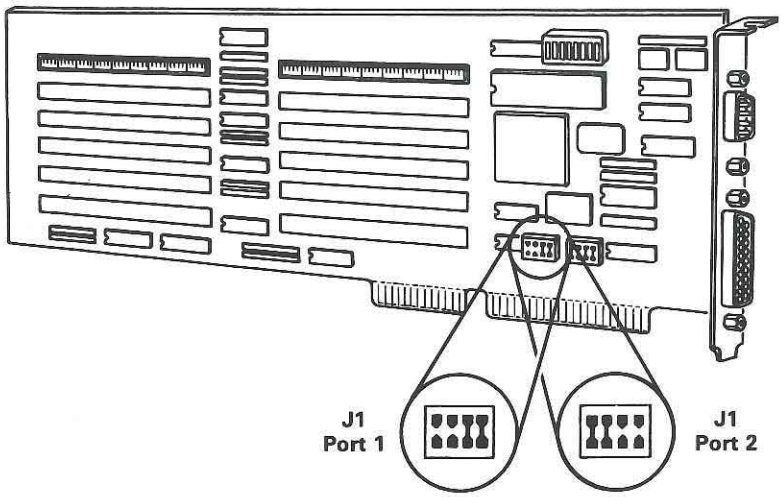
The serial portion of the adapter has a controller that provides the following functions:

- Adds or deletes standard, asynchronous-communications bits to or from a serial data stream
- Provides full, double buffering, which eliminates the need for precise synchronization
- Provides a programmable baud-rate generator
- Provides modem controls (CTS, RTS, DSR, DTR, RI, and CD).

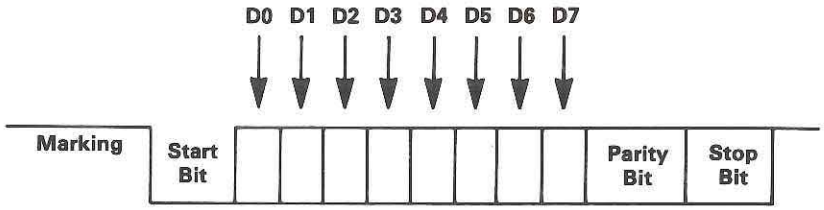
Communications Application

The serial output port may be addressed as either communications port 1 or communications port 2 as defined by jumper J1 (see the following figure). In this section hex addresses begin with an X which can be either a 3 for communications port 1 (interrupt level 4) or 2 for communications port 2 (interrupt level 3).

Note: I/O enable switch 8 must be set.



The data format will be as follows:



Data bit 0 is the first bit to be sent or received. The controller automatically inserts the start bit, the correct parity bit (1, 1.5, or 2, depending on the command in the line-control register).

Controller Specifications

The following describes the function of controller input/output signals.

Input Signals

–Clear to Send: (–CTS), Pin 36—The '–CTS' signal is a modem-control function input, the condition of which can be tested by the processor by reading bit 4 (CTS) of the modem status register. Bit 0 (DCTS) of the modem status register indicates if the '–CTS' input has changed state since the previous reading.

Note: Whenever the CTS bit of the modem status register changes state, an interrupt is generated if the modem-status interrupt is enabled.

–Data Set Ready: (–DSR), Pin 37—When low, indicates the modem or data set is ready to establish the communications link and transfer data with the controller. The '–DSR' signal is a modem-control function input, the condition of which can be tested by the processor reading bit 5 (DSR) or the modem status register. Bit 1 (DDSR of the modem status register indicates if the '–DSR' input has changed since the previous reading.

> **Note:** Whenever the DSR bit of the modem status register changes state, an interrupt is generated if the modem-status interrupt is enabled.

–Data Carrier Detect: (–DCD), Pin 38—When low, indicates the modem or data set detected a data carrier. The '–DCD' signal is a modem-control function input, the condition of which can be tested by the processor reading bit 7 (DCD) of the modem status register. Bit 3 (DCD) of the modem status register indicates if the '–DCD' input has changed state since the previous reading.

> **Note:** Whenever the DCD bit of the modem status register changes state, an interrupt is generated if the modem status interrupt is enabled.

–Ring Indicator: (–RI), Pin 39—When low, indicates the modem or data set detected a telephone ringing signal. The '–RI' signal is a modem-control function input, the condition of which can be tested by the processor reading bit 6 (RI) of the modem status register. Bit 2 (TERI) of the modem status register indicates if the '–RI' input has changed from an active to an inactive state since the previous reading.

> **Note:** Whenever the RI bit of the modem status register changes from an inactive state to an active state an interrupt is generated if the modem-status interrupt is enabled.

VCC Pin 40—+5 Vdc supply.

VSS Pin 20—Ground (0 Vdc) reference.

Output Signals

–Data Terminal Ready: (–DTR), Pin 33—When active, informs the modem or data set that the controller is ready to communicate. The 'DTR' output signal can be set to an active level by programming bit 0 (DTR) of the modem control register to an active level. The '–DTR' signal is set inactive upon a master reset operation.

–Request to Send: (–RTS), Pin 32—When active, informs the modem or data set that the controller is ready to send data. The '–RTS' output signal can be set to an active level by programming bit 1 (RTS) of the modem control register to an active level. The '–RTS' signal is set inactive upon a master reset operation.

–Output 1: (–OUT 1), Pin 34—User-designated output that can be set to an active level by programming bit 2 (–OUT 1) of the modem control register to an inactive level. The '–OUT 1' signal is set inactive upon a master reset operation. Pin 34 is connected to an active source.

–Output 2: (–OUT 2), Pin 31—User-designated output that can be set to an active level by programming bit 3 (–OUT 2) of the modem control register to an inactive level. The '–OUT 2' signal is set inactive upon a master reset operation. Pin 31 controls interrupts to the system.

Controller-Accessible Registers

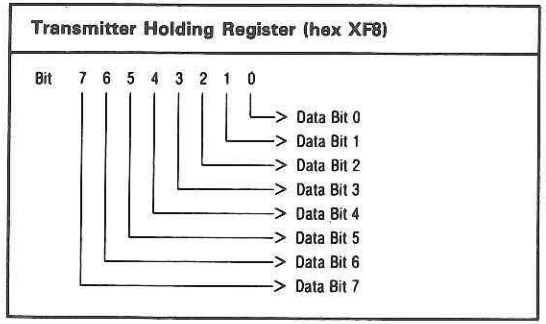
The controller has a number of accessible registers. The system programmer may gain access to or control any of the controller registers through the microprocessor. These registers are used to control the controller's operations and to transmit and receive data. The X in the register address determines the port selected; 3 is for port 1 and 2 is for port 2.

Specific registers are selected according to the following figure:

I/O Address	Register Selected	DLAB State
XF8	TX buffer	0 (write)
XF8	RX buffer	0 (read)
XF8	Divisor Latch LSB	1
XF9	Divisor Latch MSB	1
XF9	Interrupt Enable Register	0
XFA	Interrupt Identification Register	
XFB	Line Control Register	
XFC	Modem Control Register	
XFD	Line Status Register	
XFE	Modem Status Register	
XFF	Reserved	

Controller-Accessible Registers

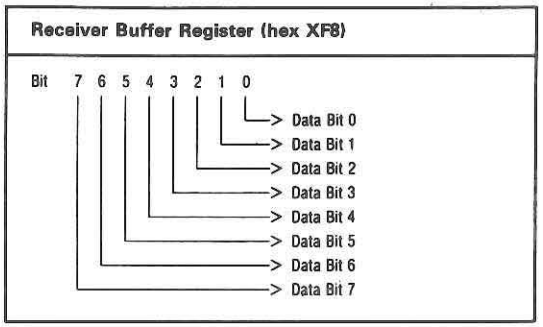
Transmitter Holding Register (Hex XF8): The transmitter holding register (THR) contains the character to be sent.



Transmitter Holding Register

Bit 0 is the least-significant bit and the first bit sent serially.

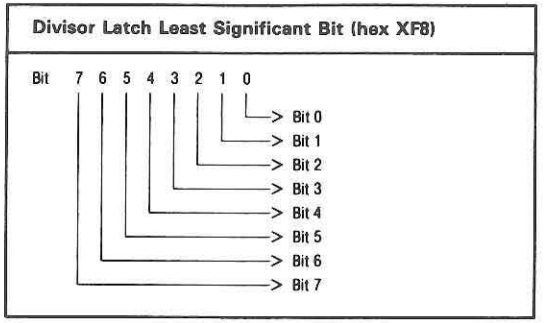
Receiver Buffer Register (Hex XF8): The receiver buffer register (RBR) contains the received character.



Receiver Buffer Register

Bit 0 is the least-significant bit and the first bit received serially.

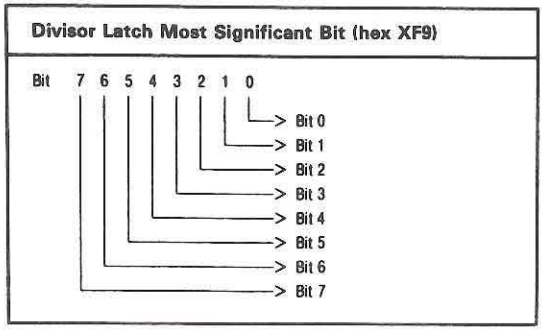
Divisor Latch LSB (Hex XF8)



Divisor Latch Least Significant Bit

Information about this register may be found under "Programmable Baud Rate Generator" later in this section.

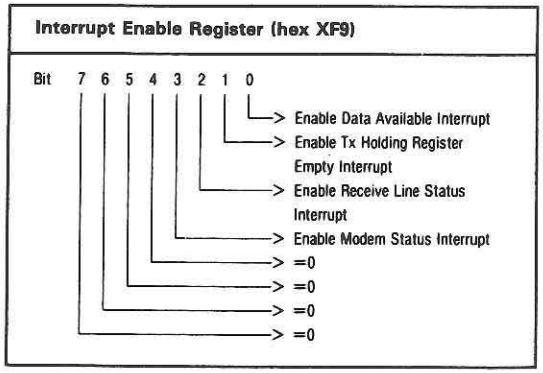
Divisor Latch MSB (Hex XF9)



Divisor Latch Most Significant Bit

Information about this register may be found under ''Programmable Baud Rate Generator'' later in this section.

Interrupt Enable Register (Hex XF9): This 8-bit register allows the four types of controller interrupts to separately activate the 'chip-interrupt' (INTRPT) output signal. The interrupt system can be totally disabled by resetting bits 0 through 3 of the interrupt enable register (IER). Similarly, by setting the appropriate bits of this register to logical 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the 'IER' and the active 'INTRPT' output from the chip. All other system functions operate normally, including the setting of the line-status and modem-status registers.



Interrupt Enable Register

Bit 0 When set to logical 1, enables the received-data-available interrupt.

Bit 1 When set to logical 1, enables the transmitter-holding-register-empty interrupt.

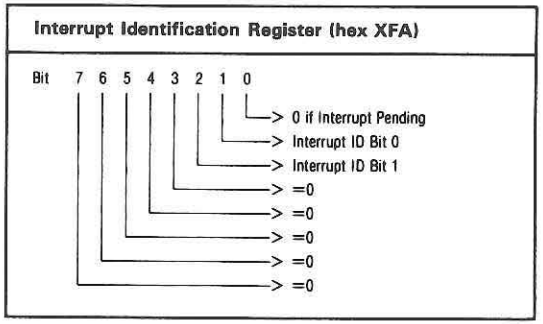
Bit 2 When set to logical 1, enables the receiver-line-status interrupt.

Bit 3 When set to logical 1, enables the modem-status interrupt.

Bits 4-7 These four bits are always logical 0.

Interrupt Identification Register (Hex XFA): The controller has an on-chip interrupt capability that makes communications possible with all of the currently popular microprocessors. In order to minimize programming overhead during data character transfers, the controller prioritizes interrupts into four levels: receiver line status (priority 1), received data ready (priority 2), transmitter holding register empty (priority 3), and modem status (priority 4).

Information about a pending prioritized interrupt is stored in the interrupt identification register (IIR). (See the figure ''Interrupt Control Functions,'' later.) The IIR, when addressed during priority, and no other interrupts are acknowledged until the processor services that particular interrupt.



Interrupt Identification Register

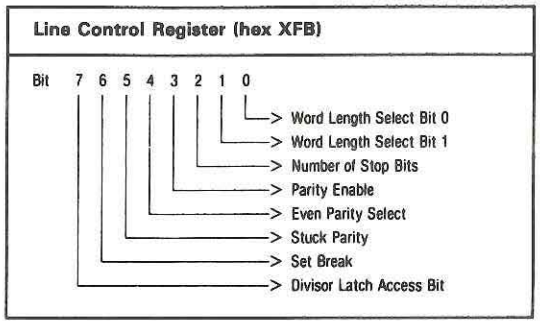
Bit 0 This bit can be used in either hard-wired, prioritized, or polled conditions to indicate if an interrupt is pending. When bit 0 is logical 0, an interrupt is pending, and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is logical 1, no interrupt is pending, and polling (if used) continues.

Bits 1-2 These two bits identify the pending interrupt that has the highest priority interrupt pending, as shown in the following figure.

Bits 3-7 These five bits are always logical 0.

Interrupt ID Register			Interrupt Set And Reset Functions			
Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Control
0	0	0	–	None	None	–
1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
1	0	0	Second	Received Data Available	Receiver Data Available	Reading the Receiver Buffer Register
0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR (if source of interrupt) or writing into the THR
0	0	0	Fourth	Modem Status	Clear to Send or Data Set Ready or Ring Indicator or Received Line Signal Detect	Reading the Modem Status Register

Line-Control Register (Hex XFB): The system programmer specifies the format of the asynchronous data communications exchange through the line control register. In addition to controlling the format, the programmer may retrieve the contents of the line control register for inspection. This feature simplifies system programming and eliminates the need to store line characteristics separately in system memory.



Line Control Register

Bits 0, 1 These two bits specify the number of bits in each serial character that is sent or received. The encoding of bits 0 and 1 is as follows:

Bit 1	Bit 2	Word Length (Bits)
0	0	5
0	1	6
1	0	7
1	1	8

Word Length

Bit 2 This bit specifies the number of stop bits in each serial character that is sent or received. If bit 2 is a logical 0, one stop bit is generated or checked in the data sent or received. If bit 2 is logical 1 when a 5-bit word length is selected through bits 0 and 1, 1-1/2 stop bits are generated or checked. If bit 2 is logical 1 when either a 6-, 7-, or 8-bit word length is selected, two stop bits are generated or checked.

Bit 3 This bit is the parity-enable bit. When bit 3 is logical 1, a parity bit is generated (transmit data) or checked (receive data) between the last data word and stop bit of the serial data. (The parity bit is used to produce an even or odd number of 1's when the data-word bits and parity bit are summed.)

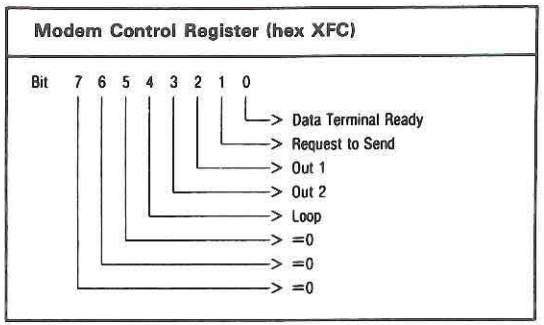
Bit 4 This bit is the even-parity-select bit. When bit 3 is a logical 1 and bit 4 is a logical 0, an odd number of logical 1's is sent or checked in the data word bits and parity bit. When both bit 3 and bit 4 are a logical 1, an even number of bits is sent or checked.

Bit 5 This bit is the stuck-parity bit. When bit 3 is a logical 1 and bit 5 is a logical 1, the parity bit is sent and then detected by the receiver as a logical 0, if bit 4 is a logical 1, or as a logical 1 if bit 4 is a logical 0.

Bit 6 This bit is the set-break control bit. When bit 6 is set to a logical 1, the serial output (SOUT) is forced to the spacing (logical 0) state and remains there regardless of other transmitter activity. The set-break is disabled by setting bit 6 to logical 0. This feature enables the microprocessor to select a specific terminal in a computer communications system.

Bit 7 This bit is the divisor-latch access bit (DLAB). It must be set high (logical 1) to gain access to the divisor latches of the baud-rate generator during a read or write operation. It must be set low (logical 0) to gain access to the receiver buffer, the transmitter holding register, or the interrupt enable register.

Modem Control Register (Hex XFC): This 8-bit register controls the data exchange with the modem or data set (an external device acting as a modem).



Modem Control Register

Bit 0 This bit controls the '–data terminal ready' (–DTR) output. When bit 0 is set to logical 1, the –DTR output is forced active. When bit 0 is reset to logical 0, the '–DTR' output is forced inactive.

Bit 1 This bit controls the '–request-to-send' (–RTS) output. Bit 1 affects the '–RTS' output in the same way bit 0 affects the '–DTR' output.

Bit 2 This bit controls the '–Output 1' (–OUT 1) signal, which is a spare the programmer can use. Bit 2 affects the '–OUT 1' output in the same way bit 0 affects the '–DTR' output.

Bit 3 This bit controls the '–Output 2' (–OUT 2) signal, which is a spare the programmer can us. Bit 3 affects the '–OUT 2' output in the same way bit 0 affects the '–DTR' output.

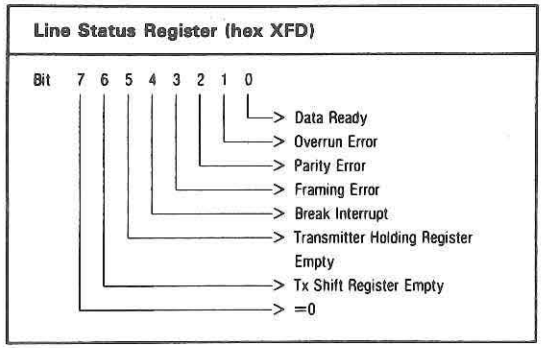
Bit 4 This bit provides a loopback feature for diagnostic testing of the controller. When bit 4 is set to logical 1, the following occur: the 'transmitter serial output' (SOUT) is set to the active state, the 'receiver serial input' (SIN) is disconnected; the output of the transmitter shift register is ''looped back'' to the receiver shift register input; the four modem-control inputs ('-CTS', '-DSR', '-RLSD', and '-RI') are disconnected; and the four modem-control outputs ('-DTR', '-RTS', '-OUT 1' and '-OUT 2') are internally connected to the four modem control inputs. In the diagnostic mode, data sent is immediately received. This feature allows the processor to verify the transmit- and receive-data paths of the controller.

In the diagnostic mode, the receiver and transmitter interrupts are fully operational, as are the modem-control interrupts. But the interrupts' sources are now the lower four bits of the modem control register (MCR) instead of the four modem-control inputs. The interrupts are still controlled by the interrupt enable register.

The controller's interrupt system can be tested by writing to the lower six bits of the line status register and the lower four bits of the modem status register. Setting any of these bits to logical 1 generates the appropriate interrupt (if enabled). Resetting these interrupts is the same as for normal controller operation. To return to normal operation the registers must be reprogrammed for normal operation, and then bit 4 of the MCR must be reset to logical 0.

Bits 5-7 These bits are permanently set to logical 0.

Line Status Register (Hex XFD): This 8-bit register provides the processor with status information about the data transfer.



Line Status Register

Bit 0 This bit is the receiver data ready (DR) indicator. It is set to logical 1 whenever a complete incoming character has been received and transferred into the receiver buffer register. Bit 0 may be reset to logical 0 by the processor either reading the data in the receiver's buffer register or writing logical 0 in it.

Bit 1 This bit is the overrun error (OE) indicator. It indicates that data in the receiver's buffer register was not read by the processor before the next character was transferred into the register, thereby destroying the previous character. The OE indicator is reset whenever the processor reads the contents of the line status register.

Bit 2 This bit is the parity error (PE) indicator and indicates the received data character does not have the correct even-parity-select bit. The PE bit is set to logical 1 upon detection of a parity error, and is reset to logical 0 whenever the processor reads the contents of the line status register.

Bit 3 This bit is the framing error (FE) indicator. It indicates the received character did not have a valid stop bit. Bit 3 is set to logical 1 whenever the stop bit following the last data bit or parity bit is detected as a zero bit (spacing level).

Bit 4 This bit is the break interrupt (BI) indicator. It is set to logical 1 whenever the received data input is held in the spacing state (logical 0) for longer than a fullword transmission time (that is, the total time of start bit + data bits + parity stop bits).

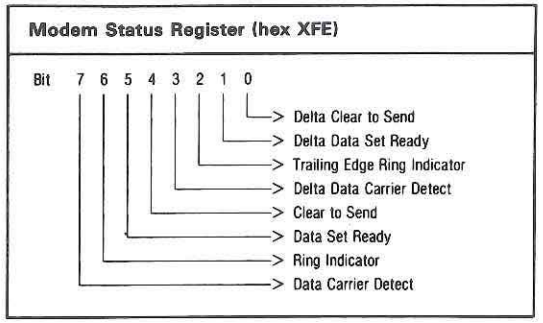
> **Note:** Bits 1 through 4 are error conditions that produce a receiver line-status interrupt whenever any of the corresponding conditions are deleted.

Bit 5 This bit is the transmitter holding register empty (THRE) indicator. It indicates the controller is ready to accept a new character for transmission. In addition, this bit causes the controller to issue an interrupt to the processor when the THRE interrupt enable is set active. The THRE bit is set to logical 1 when a character is transferred from the transmitter holding register into the transmitter shift register. It is reset to logical 0 when the processor loads the transmitter holding register.

Bit 6 This bit is the transmitter empty (TEMT) indicator. It is set to logical 1 whenever the transmitter holding request (THR) and the transmitter shift request (TSR) are both empty. It is reset to logical 0 whenever THR or TSR contains a data character.

Bit 7 This bit is permanently set to logical 0.

Modem Status Register (Hex XFE): The 8-bit MSR provides the current state of the control lines from the modem (or external device) to the processor. In addition, four bits of the MSR provide change information. These four bits are set to logical 1 whenever a control input from the modem changes state. They are reset to logical 0 whenever the processor reads this register.



Modem Status Register

Bit 0 This bit is the delta clear-to-send (DCTS) indicator. It indicates the '–CTS' input to the chip has changed state since the last time it was read by the processor.

Bit 1 This bit is the delta data-set-ready (DDSR) indicator. It indicates the '–DSR' input to the chip has changed state since the last time it was read by the processor.

Bit 2 This bit is the trailing-edge ring-indicator (TERI) detector. It indicates the '–RI' input to the chip has changed from an active condition to an inactive condition.

Bit 3 This bit is the delta data-carrier-detect (DDCD) indicator. It indicates the '–DCD' input to the chip has changed state.

> **Note:** Whenever bit 0, 1, 2, or 3 is set to a logical 1, a modem status interrupt is generated.

Bit 4 This bit is the opposite of the '–clear-to-send' (–CTS) input. If bit 4 of the MCR loop is set to a logical 1, this bit is equivalent to RTS of the MCR.

Bit 5 This bit is the opposite of the '–data-set-ready' (–DSR) input. If bit 4 of the MCR is set to a logical 1, this bit is equivalent to DTR of the MCR.

Bit 6 This bit is the opposite of the '-ring-indicator' (-RI) input. If bit 4 of the MCR is set to a logical 1, this bit is equivalent to OUT 1 of the MCR.

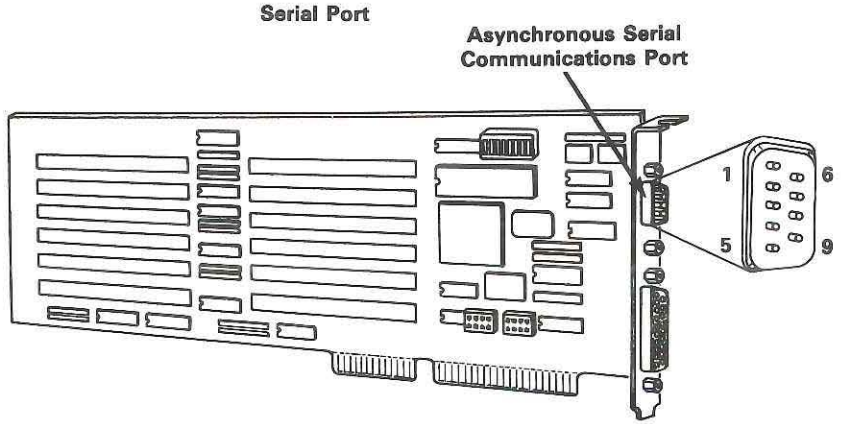
Bit 7 This bit is the opposite of the '-data-carrier-detect' (-RI) input. If bit 4 of the MCR is set to a logical 1, this bit is equivalent to OUT 2 of the MCR.

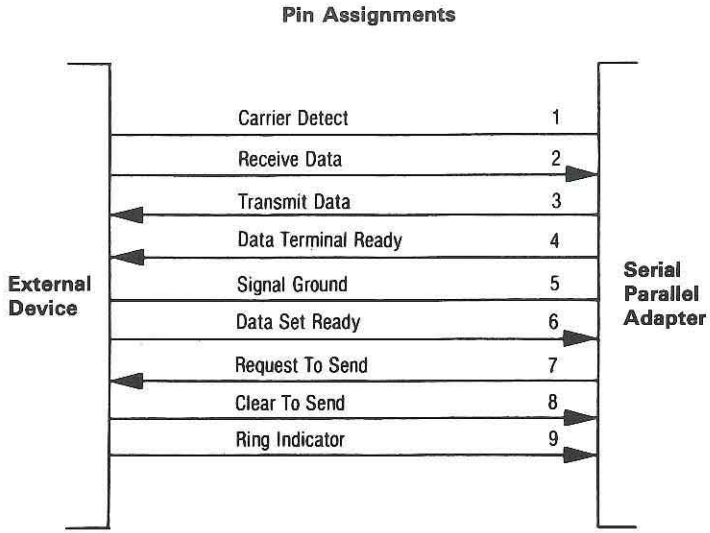
Programmable Baud-Rate Generator

The controller has a programmable baud-rate generator that can divide the clock input (1.8432 MHz) by any divisor from 1 to 655,535 or $2^{16}-1$. The output frequency of the baud-rate generator is the baud rate multiplied by 16. Two 8-bit latches store the divisor in a 16-bit binary format. These divisor latches must be loaded during setup to ensure desired operation of the baud-rate generator. When either of the divisor latches is loaded, a 16-bit baud counter is immediately loaded. This prevents long counts on the first load.

Pin Assignment for Serial Port

The following figures show the pin assignments for the serial port in a communications environment.





Notes:

Section 4. Parallel Portion of the Adapter

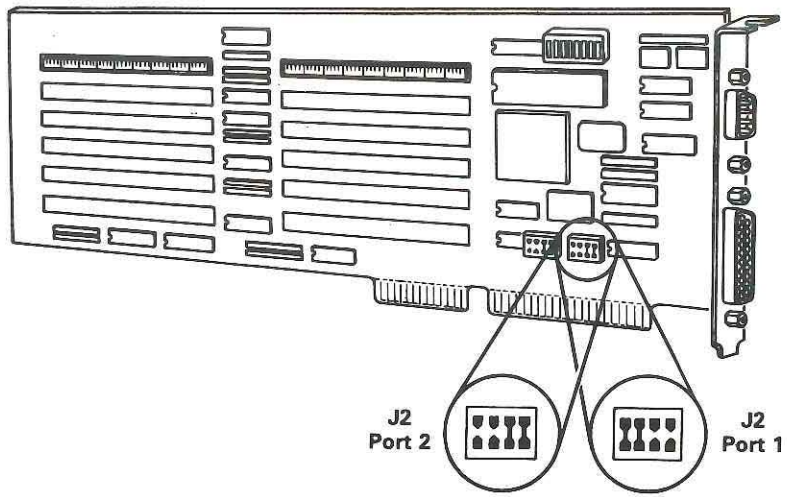
Contents

Notes:

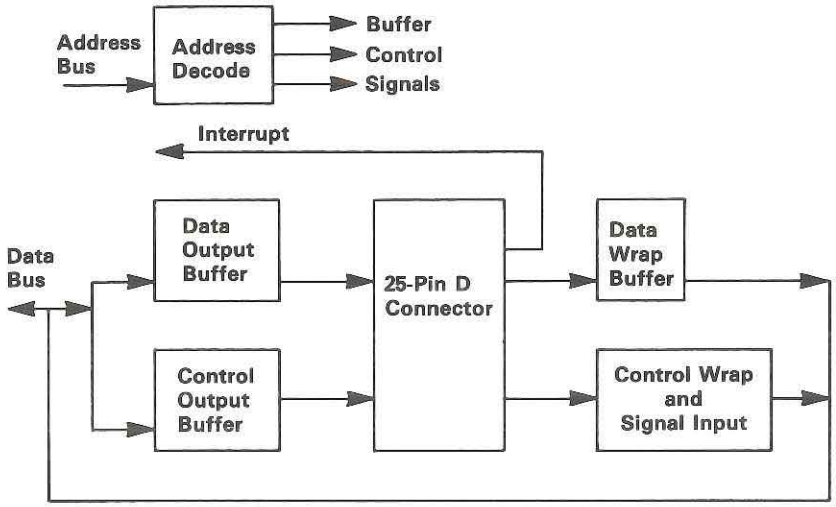
Parallel Port

The parallel portion of the adapter makes possible the attachment of various devices that accept eight bits of parallel data at standard TTL levels. The rear of the adapter has a 25-pin, D-shell connector. This port may be addressed as either parallel port 1 or 2. The port address is determined by the position of jumper J2, as shown in the following figure.

Note: I/O enable switch 8 must be set.



The following figure is a block diagram of the parallel portion of the adapter.



Parallel Portion Block Diagram

Printer Application

The following discusses the use of the parallel portion of the adapter to connect to a parallel printer. Hexadecimal addresses in this section begin with an X, which is replaced with a 3 to indicate port 1, or a 2 to indicate port 2.

Data Latch (Hex X78, X7C)

Writing to this address causes data to be stored in the printer's data buffer to the system microprocessor.

Printer Controls (Hex X7A X7E)

Printer control signals are stored at this address to be read by the system microprocessor. The following are bit definitions for this byte.

Bit 7 Not used.

Bit 6 Not used.

Bit 5 Not used.

Bit 4 +IRQ Enable—A 1 in this position allows an interrupt to occur when '-ACK' changes from true to false.

Bit 3 +SLCT IN—A 1 in this bit position selects the printer.

Bit 2 -INIT—A 0 starts the printer (50-microsecond pulse, minimum).

Bit 1 +AUTO FD XT—A 1 causes the printer to line-feed after a line is printed.

Bit 0 +STROBE—A 0.5-microsecond minimum, high, active pulse clocks data into the printer. Valid data must be present for a minimum of 0.5 microsecond before and after the strobe pulse.

Printer Status - Address X79, X7D

Printer status is stored at this address to be read by the microprocessor. The following are bit definitions for this byte.

Bit 7 -BUSY—When this signal is active, the printer is busy and cannot accept data. It may become active during data entry, while the printer is offline, during printing, when the print head is changing positions, or while in an error state.

Bit 6 -ACK—This bit represents the current state of the printer's '-ACK' signal. A zero means the printer has received the character and is ready to accept another. Normally, this signal will be active for approximately 5 microseconds before '-BUSY' stops.

Bit 5 +PE—A 1 means the printer has detected the end of paper.

Bit 4 +SLCT—A 1 means the printer is selected.

Bit 3 -Error—A 0 means the printer has encountered an error condition.

Bit 2 Unused.

Bit 1 Unused.

Bit 0 Unused.

Section 5. Specifications

Contents

Notes:

Voltage

Voltage	Current Typ.	Current Max.	Power Typ.	Power Max.	Tolerance
+5V	1.1A	2.1A	5.5W	11W	+/-5%
+12V	30MA	50MA	.38W	.63W	+/-5%
-12V	30MA	50MA	.39W	.66W	+/-10%

Temperature Variation

The adapter will operate between 16.2 and 33.3 degrees Celsius (50 and 122 degrees Fahrenheit).

Port Characteristics

The following figures list characteristics of the output driver for the parallel port.

Sink current	24 mA	Max
Source current	-2.6 mA	Max
High-level output voltage	2.4 Vdc	Min
Low-level output voltage	0.5 Vdc	Max

Parallel Data and Processor IRQ

Sink current	16 mA	Max
Source current	0.55 mA	Max
High level output voltage	5 Vdc	Minus pull-up
Low level output voltage	0.4 Vdc	Max

Parallel Control

Sink current	24 mA	Max
Source current	-15 mA	Max
High level output voltage	2.0 Vdc	Min
Low level output voltage	0.5 Vdc	Max

Parallel Processor Interface (except IRQ)

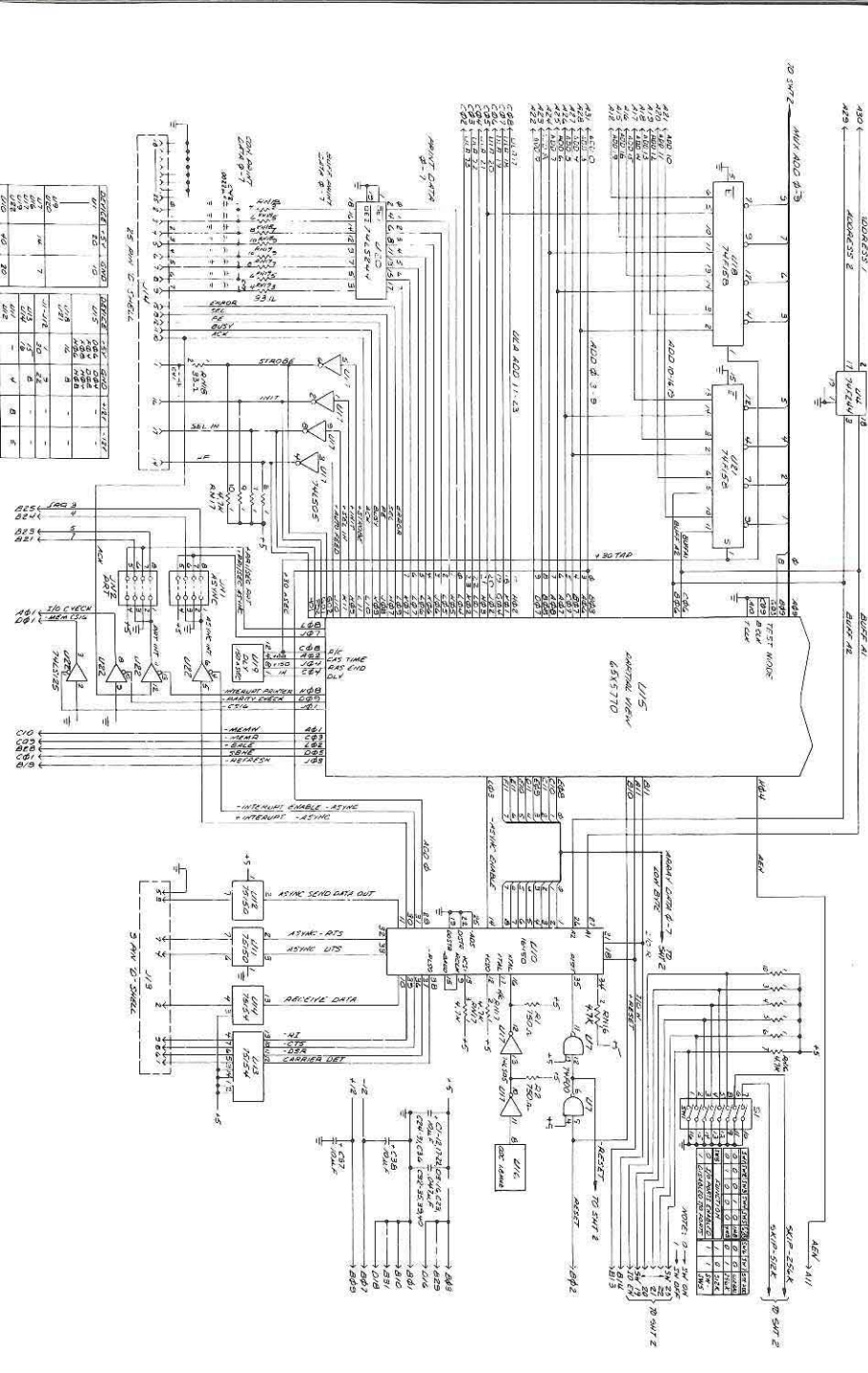
The following are the specifications for the serial interface.

Function	Condition
On	Spacing condition (binary 0, positive voltage).
Off	Marking condition (binary 1, negative voltage).

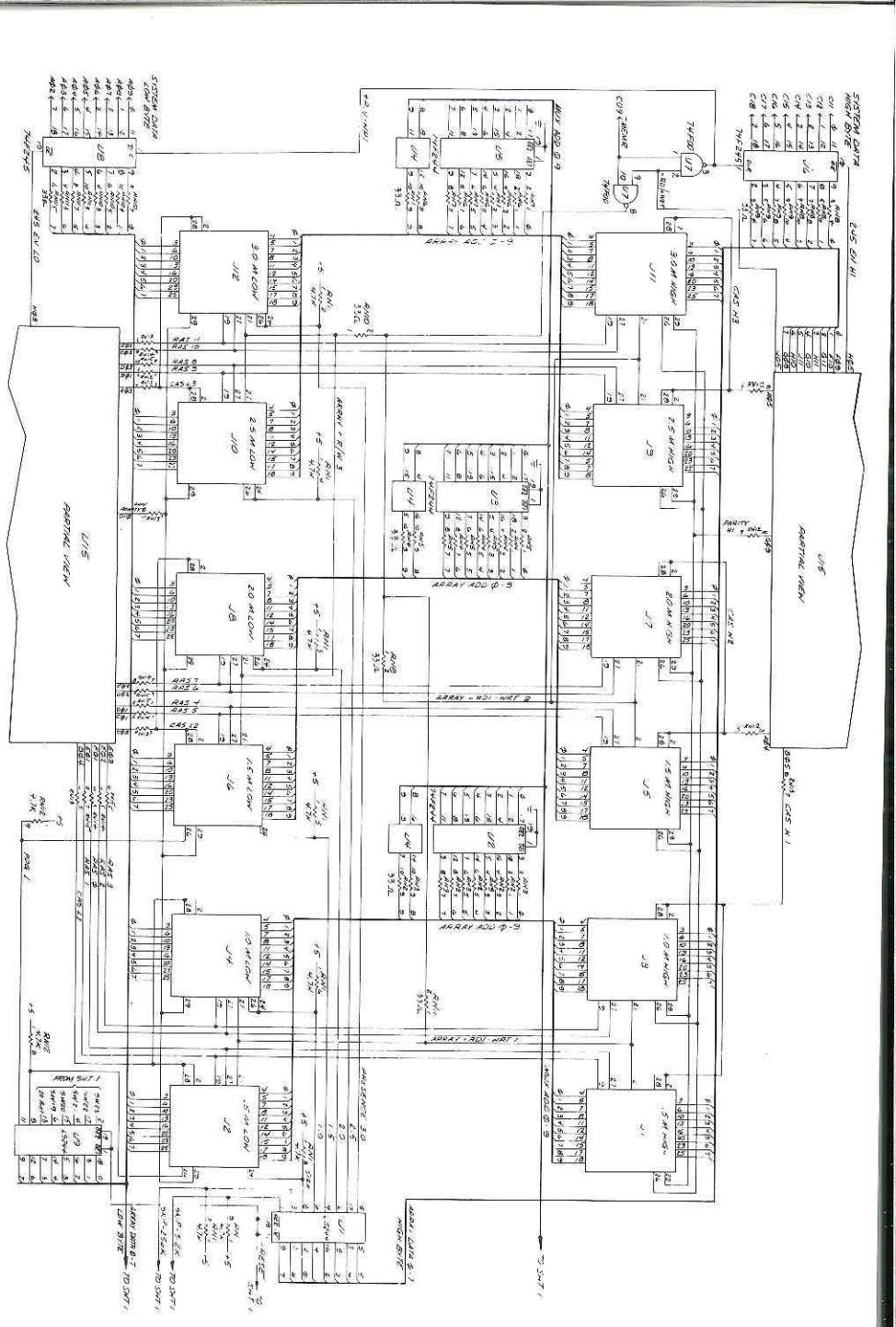
Voltage	Function
above +15 Vdc	Invalid
+3 Vdc to +15 Vdc	On
-3 Vdc to +3 Vdc	Invalid
-3 Vdc to -15 Vdc	Off
Below -15 Vdc	Invalid

Serial Port Functions

Section 6. Logic Diagrams



Enhanced Memory Expansion Adapter (Sheet 1 of 2)



Enhanced Memory Expansion Adapter (Sheet 2 of 2)

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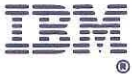

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