

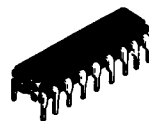
HM48416AP-12, HM48416AP-15 HM48416AP-20

16384-word × 4-bit Dynamic Random Access Memory

■ FEATURES

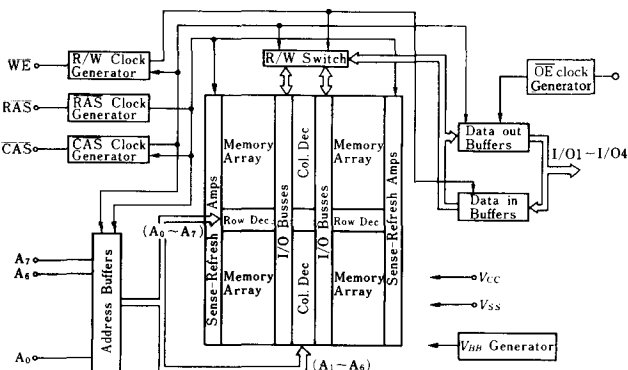
- 16384-word x 4-bit Organization
- Single 5V (±10%)
- Low Power; 303mW Active, 20mW Standby
- High speed: Access Time 120ns/150ns/200ns (max)
- Page mode capability
- Output data controlled by $\overline{\text{CAS}}$, $\overline{\text{OE}}$
- TTL compatible
- 128 refresh cycles ($A_0 \sim A_6$, 2ms)

HM48416AP-12, HM48416AP-15,
HM48416AP-20

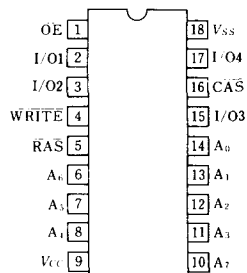


(DP-18)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

| Item | Symbol | Value | Unit |
|---|-----------|--------------|------|
| Voltage on any pin relative to V_{SS} | V_T | -1.0 to +7.0 | V |
| Supply Voltage relative to V_{SS} | V_{CC} | -1.0 to +7.0 | V |
| Short Circuit Output Current | I_{out} | 50 | mA |
| Power Dissipation | P_T | 1.0 | W |
| Operating Temperature | T_{opr} | 0 to +70 | °C |
| Storage Temperature | T_{stg} | -55 to +125 | °C |

| | |
|---------------------------|-----------------------|
| $A_0 \sim A_7$ | Address Inputs |
| $\overline{\text{CAS}}$ | Column Address Strobe |
| $I/O1 \sim I/O4$ | Data In/Data Out |
| $\overline{\text{OE}}$ | Output Enable |
| $\overline{\text{RAS}}$ | Row Address Strobe |
| $\overline{\text{WRITE}}$ | Read/Write Input |
| V_{CC} | Power (+5V) |
| V_{SS} | Ground |

■ RECOMMENDED DC OPERATING CONDITIONS ($T_a = 0$ to +70°C)

| Item | Symbol | min | typ | max | Unit |
|----------------|----------|------|-----|-----|------|
| Supply Voltage | V_{CC} | 4.5 | 5.0 | 5.5 | V |
| | V_{SS} | 0 | 0 | 0 | V |
| Input Voltage | V_{IH} | 2.4 | - | 6.5 | V |
| | V_{IL} | -1.0 | - | 0.8 | V |

Note All voltages referenced to V_{SS} .

■ DC ELECTRICAL CHARACTERISTICS ($T_a=0$ to 70°C , $V_{CC}=5\text{V}\pm 10\%$, $V_{SS}=0\text{V}$)

| Parameter | Symbol | HM48416AP-12 | | HM48416AP-15 | | HM48416AP-20 | | Unit | Notes |
|---|-----------|--------------|----------|--------------|----------|--------------|----------|---------------|-------|
| | | min | max | min | max | min | max | | |
| Operating Current (RAS, CAS Cycling; $t_{RC}=\text{min}$) | I_{CC1} | - | 60 | - | 55 | - | 45 | mA | 1, 2 |
| Standby Current (RAS= V_{IH} , Dout=High Impedance) | I_{CC2} | - | 3.5 | - | 3.5 | - | 3.5 | mA | |
| Refresh Current (RAS Cycling, CAS= V_{IH} , $t_{RC}=\text{min}$) | I_{CC3} | - | 42 | - | 38 | - | 33 | mA | 2 |
| Standby Current (RAS= V_{IH} , Dout Enable) | I_{CC5} | - | 5.5 | - | 5.5 | - | 5.5 | mA | 1 |
| Page Mode Current (RAS= V_{IL} , CAS Cycling; $t_{PC}=\text{min}$) | I_{CC6} | - | 42 | - | 38 | - | 33 | mA | 1, 2 |
| Input Leakage ($0 < V_{in} < 6.5\text{V}$) | I_{LI} | -10 | 10 | -10 | 10 | -10 | 10 | μA | |
| Output Leakage (Dout is disabled, $0 < V_{out} < 5.5\text{V}$) | I_{LO} | -10 | 10 | -10 | 10 | -10 | 10 | μA | |
| Output Levels High ($I_{out}=-5\text{mA}$) | V_{OH} | 2.4 | V_{CC} | 2.4 | V_{CC} | 2.4 | V_{CC} | V | |
| Output Levels Low ($I_{out}=4.2\text{mA}$) | V_{OL} | 0 | 0.4 | 0 | 0.4 | 0 | 0.4 | V | |

Notes) 1. I_{CC} depends on output loading condition when the device is selected, I_{CC} max is specified at the output open condition.

2. Current depends on cycle rate: maximum current is measured at the fastest cycle rate.

■ CAPACITANCE ($V_{CC}=5\text{V}\pm 10\%$, $T_a=25^\circ\text{C}$)

| Parameter | Address | Symbol | typ | max | Unit | Notes |
|--------------------|---------------------|-----------|-----|-----|------|-------|
| Input Capacitance | | C_{in1} | - | 5 | pF | 1 |
| | RAS, CAS, WRITE, OE | C_{in2} | - | 10 | pF | 1 |
| Output Capacitance | Data In/Data out | $C_{I/O}$ | - | 10 | pF | 1, 2 |

Notes) 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.

2. CAS= V_{IH} to disable Dout.

■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

($T_a=0$ to 70°C , $V_{CC}=5\text{V}\pm 10\%$, $V_{SS}=0\text{V}$)^{1), 10)}

| Parameter | Symbol | HM48416AP-12 | | HM48416AP-15 | | HM48416AP-20 | | Unit | Note |
|--|------------|--------------|-------|--------------|-------|--------------|-------|------|------|
| | | min | mas | min | max | min | max | | |
| Random Read or Write Cycle Time | t_{RC} | 230 | - | 260 | - | 330 | - | ns | |
| Read-Write Cycle Time | t_{RWC} | 320 | - | 360 | - | 450 | - | ns | |
| Page Mode Cycle Time | t_{PC} | 130 | - | 145 | - | 190 | - | ns | |
| Access Time from RAS | t_{RAC} | - | 120 | - | 150 | - | 200 | ns | 2, 3 |
| Access Time from CAS | t_{CAC} | - | 60 | - | 75 | - | 100 | ns | 3, 4 |
| Output Buffer Turn-off Delay referenced to CAS | t_{OFF1} | - | 35 | - | 40 | - | 50 | ns | 5 |
| Transition Time (Rise and Fall) | t_T | 3 | 35 | 3 | 35 | 3 | 50 | ns | 6 |
| RAS Precharge Time | t_{RP} | 100 | - | 100 | - | 120 | - | ns | |
| RAS Pulse Width | t_{RAS} | 120 | 10000 | 150 | 10000 | 200 | 10000 | ns | |
| CAS Pulse Width | t_{CAS} | 60 | 10000 | 75 | 10000 | 100 | 10000 | ns | |
| RAS to CAS Delay Time | t_{RCD} | 25 | 60 | 25 | 75 | 30 | 100 | ns | 7 |
| RAS Hold Time | t_{RSH} | 60 | - | 75 | - | 100 | - | ns | |
| CAS Hold Time | t_{CSH} | 120 | - | 150 | - | 200 | - | ns | |
| CAS to RAS Precharge Time | t_{CRP} | -10 | - | -10 | - | -10 | - | ns | |
| Row Address Set-up Time | t_{ASR} | 0 | - | 0 | - | 0 | - | ns | |
| Row Address Hold Time | t_{RAH} | 15 | - | 15 | - | 20 | - | ns | |
| Column Address Set-up Time | t_{ASC} | 0 | - | 0 | - | 0 | - | ns | |
| Column Address Hold Time | t_{CAH} | 20 | - | 25 | - | 30 | - | ns | |
| Column Address Hold Time referenced to RAS | t_{AR} | 80 | - | 100 | - | 130 | - | ns | |
| Write Command Set-up Time | t_{WCS} | 0 | - | 0 | - | 0 | - | ns | 8 |
| Write Command Hold Time | t_{WCH} | 40 | - | 45 | - | 55 | - | ns | |

(to be continued)

| Parameter | Symbol | HM48416AP-12 | | HM48416AP-15 | | HM48416AP-20 | | Unit | Note |
|---|------------|--------------|-----|--------------|-----|--------------|-----|------|------|
| | | min | max | min | max | min | max | | |
| Write Command Hold Time referenced to RAS | t_{WCR} | 100 | — | 120 | — | 155 | — | ns | |
| Write Command Pulse Width | t_{WP} | 40 | — | 45 | — | 55 | — | ns | |
| Write Command to RAS Lead Time | t_{RWL} | 40 | — | 45 | — | 55 | — | ns | |
| Write Command to CAS Lead Time | t_{CWL} | 40 | — | 45 | — | 55 | — | ns | |
| Data-in Set-up Time | t_{DS} | 0 | — | 0 | — | 0 | — | ns | 9 |
| Data-in Hold Time | t_{DH} | 40 | — | 45 | — | 55 | — | ns | 9 |
| Data-in Hold Time referenced to RAS | t_{DHR} | 100 | — | 120 | — | 155 | — | ns | |
| Read Command Set-up Time | t_{RCS} | 0 | — | 0 | — | 0 | — | ns | |
| Read Command Hold Time referenced to CAS | t_{RCH} | 0 | — | 0 | — | 0 | — | ns | |
| Read Command Hold Time referenced to RAS | t_{RRH} | 10 | — | 10 | — | 10 | — | ns | |
| Refresh Period | t_{REF} | — | 2 | — | 2 | — | 2 | ms | |
| CAS to WE Delay Time | t_{CWD} | 105 | — | 125 | — | 160 | — | ns | 8 |
| RAS to WE Delay Time | t_{RWD} | 165 | — | 200 | — | 260 | — | ns | 8 |
| CAS Precharge Time (for Page-mode Cycle Only) | t_{CP} | 60 | — | 60 | — | 80 | — | ns | |
| CAS Precharge Time | t_{CPN} | 35 | — | 40 | — | 50 | — | ns | |
| RAS Precharge to CAS Hold Time | t_{RPC} | 0 | — | 0 | — | 0 | — | ns | |
| Access Time from OE | t_{OAC} | — | 35 | — | 40 | — | 50 | ns | 3 |
| Output Buffer Turn-off Delay referenced to OE | t_{OFF2} | — | 35 | — | 40 | — | 50 | ns | 5 |
| OE to Data-in Delay Time | t_{ODD} | 35 | — | 40 | — | 50 | — | ns | 11 |

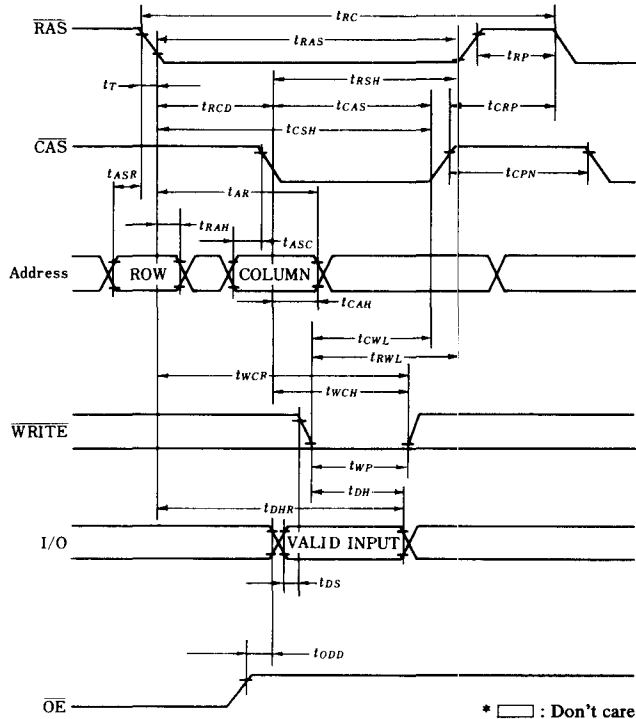
Notes:

1. AC measurements assume $t_T = 5ns$.
2. Assumes that $t_{RCD} \geq t_{RCD} (max)$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geq t_{RCD} (max)$.
5. $t_{OFF1} (max)$ and $t_{OFF2} (max)$ define the time at which the output achieves the open circuit condition.
6. $V_{IH} (min)$ and $V_{IL} (max)$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
7. Operation within the $t_{RCD} (max)$ limit insures that $t_{RAC}(max)$ can be met, $t_{RCD} (max)$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{RCD} (max)$ limit, then access time is controlled exclusively by t_{CAC} .
8. t_{WCS} , t_{CWD} and t_{RWD} are not restrictive operating parameters.

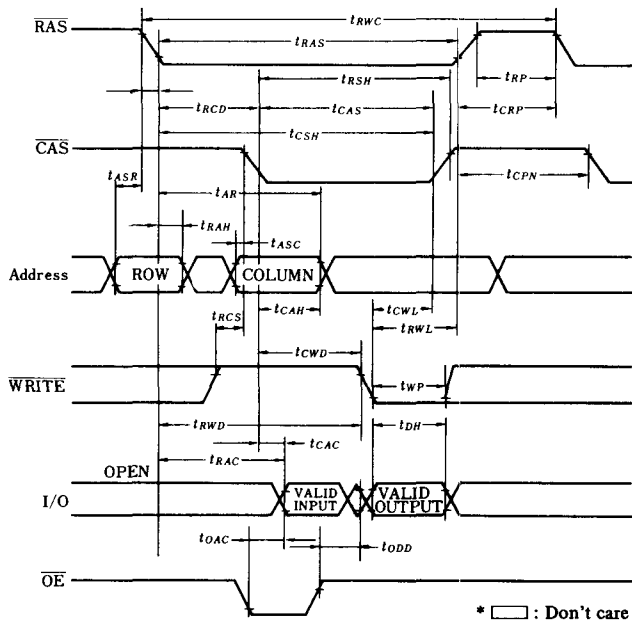
They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS} (min)$, the cycle is an early write cycle and the data output pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD} (min)$ and $t_{RWD} \geq t_{RWD} (min)$ the cycle is a read-write cycle and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

9. These parameters are referenced to CAS leading edge in early write cycles and to WE leading edge in delayed write or read-modify-write cycles.
10. An initial pause of 100 μs is required after power-up followed by a minimum of 8 initialization cycles.
11. In delayed write or read-modify-write cycles, OE must disable output buffers prior to applying data to the device.

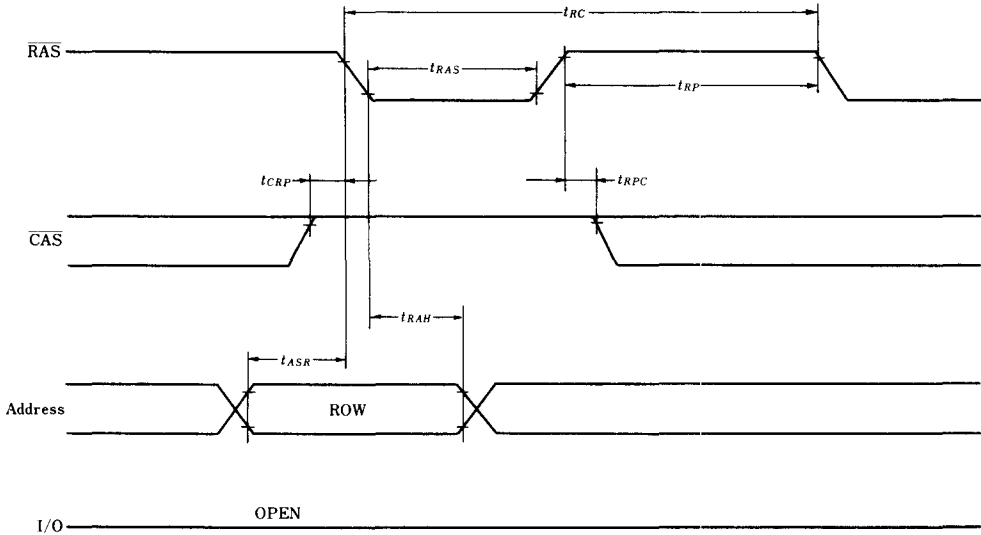
● Delayed Write Cycle



● Read Modify Write Cycle



● RAS Only Refresh Cycle



*OE, WE : Don't care
□ : Don't care