Technical Information Manual

IntelliStation Z Pro
Professional Workstation (Type 6865)

Note

Before using this information and the product it supports, be sure to read the general information under Appendix E, “Notices and Trademarks” on page 58.

Second Edition (January 1999)

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Preface

This *Technical Information Manual* provides information on IBM IntelliStation Z Pro (Type 6865) computers. The manual provides in-depth information on how these computers work, and is intended for developers who want to provide hardware and software products to operate with these computers. Users of this publication should have an understanding of computer architecture and programming concepts.

Manual Style

In this manual, the use of the letter “h” indicates a hexadecimal number. Also, when numerical modifiers such as “K,” “M,” and “G” are used, they typically indicate powers of 2, not powers of 10. For example, 1 KB equals 1 024 bytes (2^{10}), 1 MB equals 1 048 576 bytes (2^{20}), and 1 GB equals 1 073 741 824 bytes (2^{30}).

When expressing hard disk storage capacity, powers of 10 are used (1 MB equals 1 000 KB, or 1 000 000 bytes). The value is determined by counting the number of sectors and assuming that every sector equals 512 bytes. Depending on the operating system and other system requirements, the storage capacity available to the user might vary.

Warning: The term *reserved* describes certain signals, bits, and registers that should not be changed. Use of reserved areas can cause compatibility problems, loss of data, or permanent damage to the hardware. When the contents of a register are changed, the state of the reserved bits must be preserved. When possible, read the register first and change only the bits that must be changed.

Some signals are abbreviated. A minus sign in front of a signal indicates that the signal is active low. No sign in front of a signal indicates that the signal is active high.

Related Publications

In addition to this manual, the following IBM publications provide information about the operation of the IntelliStation Z Pro (Type 6865). To order these publications, call 1-800-879-2755 in the U.S. and Puerto Rico. In other countries, contact an IBM reseller or IBM marketing representative.

- *IntelliStation Z Pro User Guide*
  This publication contains the following:
  - Instructions for setting up your computer
  - Instructions for configuring, operating, and maintaining your computer
  - Information on diagnosing and solving computer problems and how to get help and service
  - Warranty information
- *Installing Options in Your IntelliStation Z Pro*
  This online publication (provided on the Ready-to-Configure Utility program CD (RTC-CD) that comes with your computer) includes information for adding memory, adapters, drives, and other options to your computer. It is also available as a printable file (.PDF) from the World Wide Web at:

  `http://www.pc.ibm.com/support`
- *Understanding Your IntelliStation Z Pro*
  This publication includes general information about using computers and detailed information about the features of IntelliStation Z Pro computers. The publication is available on the *Ready-to-Configure Utility Program CD* that comes with the computer. If the computer comes with IBM-preinstalled software, this publication is also included in the preinstalled software package.
- *About Your Software*
  This publication (provided only with computers that have IBM-preinstalled software) contains information about the preinstalled software package.
- *Ready-to-Configure Utility Program CD*
  This publication contains information about the *Ready-to-Configure Utility Program CD* that comes with IntelliStation Z Pro computers. The publication also contains instructions for starting the CD.
- *Adaptec SCSI Documentation*
  This documentation, which is provided on the *Ready-to-Configure Utility Program CD* that comes with IntelliStation Z Pro computers, includes information on the SCSI interface, including instructions for installing and configuring SCSI devices.
- *Hardware Maintenance Manual*
  This publication contains information on IntelliStation Z Pro computers for trained service technicians. It can be found at http://www.pc.ibm.com/us/intellistation/tech_library.html on the World Wide Web. The publication can also be ordered from IBM. To purchase a copy, refer to the "Getting Help, Service, and Information" section in the *IntelliStation Z Pro User Guide*.
- *Compatibility Report*
  This publication contains information about compatible hardware and software for IntelliStation Z Pro computers. The publication is available at http://www.pc.ibm.com/us/intellistation/tech_library.html on the World Wide Web.

Chapter 1. System Overview

The IntelliStation Z Pro is a versatile product designed to provide state-of-the-art computing power with room for future growth.

Hardware Features

The major features of IntelliStation Z Pro computers are:

- Intel® Pentium® Xeon™ microprocessor with MMX™ technology
- Support for up to 2048 MB (2 GB) of system memory (SDRAM)
- Up to 2 MB L2 cache memory integrated into microprocessor
- PCI, ISA, and AGP buses
- Busmaster Ultra DMA-33 IDE controller
- Preinstalled Adaptec SCSI Card 2940U2W
- EIDE, Ultra Wide SCSI, or Ultra SCSI hard disk drive
- IDE CD-ROM drive
- 3.5-inch, 1.44 MB diskette drive
- One of the following graphics adapters is preinstalled:
  - Matrox AGP graphics adapter
  - Intergraph PCI graphics adapter
- Integrated Crystal 4235 audio subsystem (supports SoundBlaster and Microsoft Windows Sound System applications)
- Integrated Intel EtherExpress Pro/100B Ethernet subsystem with Wake on LAN
- System Management
  - RPL (remote program load) and DHCP (dynamic host configuration protocol)
  - Integrated Wake on LAN controller
  - Alert on LAN
  - Automatic power-on startup sequence
  - Update POST and BIOS over the network
  - DMI (Desktop Management Interface) BIOS and DMI software
  - Store POST hardware test results
  - Remote reset from LAN
  - Integrated system management controller
  - Built-in system management hardware (temperature sensors, fan-speed monitor, chassis-intrusion detector, power supply and processor voltage monitor, and power-switch bypass)
- Input/Output Features
  - One 25-pin, ECP/EPP parallel port
  - Two 9-pin, 16550 UART serial ports
  - Two 4-pin, USB (universal serial bus) ports
  - One 6-pin, keyboard port
  - One 6-pin, mouse port
  - One 15-pin, monitor port (on graphics adapter)
  - Three 3.5-mm, audio jacks (line out, line in, and microphone)
  - One Ethernet RJ-45 port
- Expansion
  - Seven drive bays (three of which are occupied by the preinstalled floppy, hard disk, and CD-ROM drives)
  - Seven expansion slots (five dedicated PCI, one shared ISA/PCI, and one dedicated AGP). One of these slots is occupied by the preinstalled graphics adapter.
  - Second microprocessor socket
  - Four memory sockets (one of which is occupied by preinstalled memory)

  – Support for additional internal and external SCSI devices (The number of internal devices that can be installed is limited by the number of available drive bays and power and cooling requirements.)

Several model variations are available for IntelliStation Z Pro computers. The following list describes some of the ways in which the models vary:

- Microprocessor speed
- Hard disk type and capacity
- Amount of system memory preinstalled
- Type of video adapter preinstalled

Software Features

This section describes the system software, device drivers, and operating system support provided with IntelliStation Z Pro computers.

System Software

System software refers to the following:

- Basic input/output system (BIOS)
- Plug and Play
- Power-on self-test (POST)
- Configuration/Setup Utility program
- Advanced Power Management (APM)
- Flash update utility program
- Diagnostic programs

BIOS

IntelliStation Z Pro computers have an IBM BIOS. Support is provided for the following features:

- PCI bus, according to the PCI BIOS Specification (Version 2.1)
- Plug and Play, according to the Plug and Play BIOS Specification (Version 1.0a)
- Advanced Power Management, according to the APM BIOS Interface Specification (Version 1.2)
- Advanced Configuration and Power Interface (ACPI) BIOS (Version 1.0a)
- System Management BIOS, according to SM BIOS Specification 2.3
- IDE LBA to allow access to hard disks with a capacity greater than 527 MB
- Intel 82440GX core chipset
- Intel Ethernet BIOS
- Crystal audio setup
- Initialization of National Semiconductor PC97307 I/O chip, with Plug and Play support
- Bootable CD-ROM
- DBCS code (for Japanese systems only)
- Wake on LAN
- RPL (Remote Program Load) and DHCP (Dynamic Host Configuration Protocol)
- Flash over LAN
- Alternate boot sequence
- Enable/disable of system board Ethernet controller

Plug and Play

IntelliStation Z Pro computers conform to the following:

- *Plug and Play BIOS Specification (Version 1.0a)*
- *Plug and Play BIOS Specification, Errata and Clarifications (Version 1.0a)*, as released by Microsoft
- *Plug and Play BIOS Extension Design Guide (Version 1.0)*
- *Guide to Integrating the Plug and Play BIOS Extensions with System BIOS (Version 1.1)*
- *Plug and Play Kit for DOS and Windows*

POST

IntelliStation Z Pro computers use IBM power-on self-test (POST) software with initialization code added for the various chips on the system board.

POST software locates any hardware problems or configuration changes. If an error occurs while POST is running, an error code in the form of a text message displays on the screen. For a description of POST error codes, see “POST Error Codes” on page 55. For further information on POST, refer to the *IntelliStation Z Pro User Guide*.

Configuration/Setup Utility Program

The Configuration/Setup Utility program provides menus for viewing and changing selections for devices and I/O ports, current date and time, start options, system security, advanced setup, ISA legacy resources, and advanced power management. The Configuration/Setup Utility program also provides system summary and product data screens which contain information specific to the computer model being used. Refer to the *IntelliStation Z Pro User Guide* for further information on the Configuration/Setup Utility program.

Advanced Power Management

Advanced Power Management (APM) is a feature that reduces power consumption when components of the computer (or the entire computer system) are not in use. When enabled, APM initiates reduced-power modes for the microprocessor, monitor, hard disk drive, or entire system after a specified period of inactivity is reached.[1]

APM is implemented in IntelliStation Z Pro computers according to the APM BIOS Interface Specification (Version 1.2). For more information on APM, refer to *Understanding Your IntelliStation Z Pro* and the *IntelliStation Z Pro User Guide*.

Advanced Configuration and Power Interface (ACPI)

IntelliStation Z Pro computers support Advanced Configuration and Power Interface (ACPI). ACPI, when enabled, allows the operating system to control the power management features of your computer. Not all operating systems support ACPI. Refer to your operating system documentation to determine if ACPI is supported.

Flash Update Utility Program

A stand-alone utility program is available to support user-initiated flash code updates. This utility program updates the BIOS code in flash memory. IntelliStation Z Pro computers also support BIOS updating over the LAN (Flash-over-LAN). The Flash-over-LAN function requires the use of the integrated system board Ethernet.

The flash update utility program is available at http://www.pc.ibm.com/us/intellistation on the World Wide Web. (Select **Support** at this Web site.) The flash update utility program is also available through the PC Company Bulletin Board Service in files that can be downloaded onto a diskette. Instructions for using the flash update utility program will be available in a README file included in the downloaded files. Refer to the *IntelliStation Z Pro User Guide* for further information.

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[1] SCSI hard disk drives do not support APM.

Diagnostic Programs

An *IBM Enhanced Diagnostics CD* comes with IntelliStation Z Pro (Type 6865) computers. The CD provides programs that you can run to diagnose hardware and some software problems. Several utility programs that provide helpful information about your computer are also included. The user interface for running these diagnostics and utilities is provided by WaterGate Software's PC Doctor.

These diagnostics help to isolate your computer hardware from software that was preinstalled (or that you have installed) on your hard disk. The programs run independent of the operating system, and *must* be run either from the CD or from a diskette that can be created from the CD or downloaded from the World Wide Web. These diagnostics are generally used when other methods are not accessible or have not been successful in isolating a problem suspected to be hardware related.

If necessary, you can also download the latest image of the diagnostics from the World Wide Web. For instructions on downloading the image and creating a bootable Enhanced Diagnostics diskette, as well as other information on the diagnostic programs that come with IntelliStation Z Pro (Type 6865) computers, refer to the *IntelliStation Z Pro User Guide*.

Device Drivers

IntelliStation Z Pro computers come with device drivers to support built-in features and several operating systems. The device drivers are preinstalled in models that come with IBM-preinstalled software. In addition, the device drivers are included on the *Ready-to-Configure Utility Program CD* that is provided with IntelliStation Z Pro computers. The device drivers are also available on the World Wide Web at http://www.pc.ibm.com/us/intellistation. (Select **Support** at this Web site.)

Operating System Support

Although a variety of operating systems can be used with IntelliStation Z Pro computers, full function is provided only with Windows NT 4.0 with Service Pack 3. Windows 95 and Windows 98 are supported but will not be preloaded. For a list of operating systems that are compatible with IntelliStation Z Pro computers, refer to the *IntelliStation Z Pro User Guide* and the IBM online compatibility report on the World Wide Web at http://www.pc.ibm.com/us/intellistation/tech_library.html.

Note: Windows NT 4.0 and various support programs are preinstalled in some IntelliStation Z Pro computers. Refer to *About Your Software* for a detailed description of the preinstallation package. Also, a *Ready-to-Configure Utility Program CD* is included with all models. The *Ready-to-Configure Utility Program CD* contains applications and device driver support for the preinstalled operating system (if applicable), and several other operating systems.

Chapter 2. System Board Features

This section provides information about system board features. For an illustration of the system board, refer to “Physical Layout of System Board” on page 19.

For a list of features provided with IntelliStation Z Pro computers, refer to “Hardware Features” on page 1.

Microprocessor

IntelliStation Z Pro computers have an Intel Pentium Xeon microprocessor with MMX technology. This is a high-performance processor that is fully compatible with previous generations of Intel microprocessors. It has separate core supply and I/O supply voltages. A voltage regulator on the system board converts the 5.0 V provided by the power supply to the core voltage required by the microprocessor.

The Pentium Xeon microprocessor with MMX technology features the following:

- Optimization for 32-bit software
- Operation at a lower voltage level than previous microprocessors
- 64-bit data bus
- 32 KB L1 cache (split into 16 KB write-through code cache and 16 KB write-back data cache)
- 100 MHz bus speed
- Power management features
- Math coprocessor
- Support for MMX technology (boosts the processing of graphic, video, and audio data)
- Up to 2 MB L2 cache, operating at the full microprocessor core speed

More information on the Pentium Xeon processor can be found on the World Wide Web at http://www.intel.com.

The microprocessor is packaged on a card with a 330-pin edge connector.

IntelliStation Z Pro (Type 6865) computers support dual microprocessors, which means microprocessor performance can be upgraded by adding a second microprocessor to the system board. If a second microprocessor is added, the speed of the second microprocessor must be the same as that of the primary microprocessor.

For information on replacing a microprocessor, installing an upgrade, or installing a second microprocessor, refer to *Installing Options in Your IntelliStation Z Pro*.

Chip Set Control

IntelliStation Z Pro computers use the Intel 82440GX chip set. The primary functions of this chipset are:

- Provides a bridge between the PCI bus and the microprocessor bus (For information on the PCI bus, see “PCI-to-ISA Bridge.”)
- Provides a DRAM controller and datapath
- Provides an interface for the Accelerated Graphics Port (AGP)

The 82440GX module is fully compliant with *PCI Local Bus Specification (Version 2.1)*.

System Memory

The system memory interface in IntelliStation Z Pro computers is controlled by the Intel 82440GX chip set module. (Refer to “Chip Set Control” for information on this module.) There are four dual inline memory module (DIMM) sockets on the system board. The DIMM sockets are powered by +3.3 volts. This voltage allows for low-power operation and supports 64-Mbit technology. For DIMM socket pin assignments, refer to “System Memory Connectors” on page 42.

The system board supports:

- Up to 2048 MB (2 GB) of system memory
- A maximum of 512 MB of system memory in each DIMM socket
- DIMM heights up to 2.5 inches

Almost any configuration of DIMMs is acceptable. However, DIMMs must have the following characteristics:

- Must be 72-bit wide, 100 MHz, SDRAM (synchronous dynamic random access memory) DIMMs
- Must be 128, 256, or 512 MB in size (either single-sided or double-sided configurations)
- Must be industry standard, 168-pin, +3 V, serial PD type
- Must have gold-lead tabs

Also, note the following:

- Fill each DIMM connector sequentially, starting with DIMM socket 0.
- Use only registered ECC (error correcting code) DIMMs.
- EDO and nonparity DIMMs are not supported.
- Single inline memory modules (SIMMs) are not supported.

PCI-to-ISA Bridge

The PIIX4 chipset module provides the bridge between the peripheral component interconnect (PCI) and industry standard architecture (ISA) buses. The chip is used to convert PCI bus cycles to ISA bus cycles.

The PCI bus is compliant with *PCI Local Bus Specification 2.1*. The PCI bus runs at a frequency of 33 MHz. The ISA bus is permanently set to the PCI bus speed divided by four (8.33 MHz).

For information on PCI and ISA bus expansion connectors, see Appendix A, “Connector Pin Assignments” on page 32.

System I/O and Power Management

The Intel PIIX4 chipset module that provides the PCI-to-ISA bridge also provides many of the subsystems of the ISA bus. These subsystems are:

- An ISA-compatible interrupt controller that provides the function of two cascaded 82C59 interrupt controllers
- Three counters, equivalent to an 82C54 programmable interval timer
- The function of two 82C37 DMA controllers with seven independent DMA channels (four 8-bit channels and three 16-bit channels)
- Power management features

For further information on the PIIX4 chipset module, refer to “Chip Set Control” on page 7.

AGP Interface

AGP (accelerated graphics port) is a high performance interface directed at 3D graphical display applications. The AGP signals are similar to PCI bus signals with performance extensions added specifically for video functions.

AGP basically creates a preferred access port for video devices into system memory. This allows efficient use of memory resources by mapping system memory as special memory for video use only. One of the primary applications for this memory mapping is for video texture data storage. Video textures are basically templates that are stored in memory and then applied to pixel data at the time of rendering. These textures are typically used in 3D display applications. AGP allows this memory to be mapped from main memory when needed, thus providing potential for high speed 3D rendering while minimizing system cost.

The AGP hardware interface is based on the 64-bit PCI definition with the following features added:

- Support for deeply pipelined read and writes
- Demultiplexed address and data, allowing almost 100% bus efficiency
- Timing support for 133 MHz data transfer rates, yielding burst data rates of over 500 MB/sec.
- Point-to-point signaling protocol for high speed operation
- 3.3 V only operation

The AGP connector on the system board is defined as a 124-pin high density custom connector for use by AGP enabled video devices only. It *does not* support generic PCI devices. For configuration purposes, an AGP video adapter will appear as a PCI device attached to the corresponding PCI bus.

IDE Bus Master Interface

The system board incorporates a PCI-to-IDE interface that complies with the AT attachment interface. This interface includes the original IDE (ATA) interface with extensions for Ultra DMA-33. The Intel PIIX4 chipset module contains the controller for the PCI Bus Master IDE interface. The PIIX4 module allows concurrent operations on the PCI and IDE buses. (Refer to “Chip Set Control” on page 7 for further information on the PIIX4 module.)

The primary and secondary IDE buses are routed to two connectors on the system board. A total of four IDE or EIDE devices can be attached to the two IDE system board connectors using ribbon cables. (However, the number of devices that can be installed is limited by the number of available drive bays.) The IDE devices receive their power through separate, four-position power cables containing +5 V, +12 V, and ground (GND) voltage.

On each IDE connector, one device is designated as the primary (master) device, and the other device is designated as the secondary (subordinate) device. These designations are determined by switch or jumper settings on each device. A functional primary device must be present on each IDE connector for a secondary device to be recognized on that same IDE connector. Care must be taken to ensure that the jumpers on the devices installed in the system correctly identify them as either primary or secondary devices. Otherwise, some of the devices might not be recognized by the system. There is no performance impact between a primary device and a secondary device of the same type on the same IDE connector.

A bootable IDE or EIDE hard disk drive can be installed on either IDE connector. A bootable hard disk is one which has an active partition with an operating system installed on it.

PCI or ISA IDE expansion adapters are not supported.

For a list of devices that can be installed in IntelliStation Z Pro computers, refer to “Internal Drives” on page 21.

The following table shows the typical system resource assignments for the IDE interface.

Table 1. System Resource Assignments for the IDE Interface

Configuration	ROM	RAM	I/O Address (Hex)	IRQ	DMA
IDE 1	None	None	01F0-01F7, 03F6, 03F7 bits 6:0	14	None
IDE 2	None	None	0170-0177, 0376-0377	15	None

Notes:

1. IDE 1 is the default for the primary channel.
2. IDE 2 is the default for the secondary channel.

When the computer is started, the resource assignments are subject to change during POST.

Two 40-pin connectors are provided on the system board for the IDE interface. For information on connector pin assignments, see “IDE Connectors” on page 38.

USB Interface

The Intel PIIX4 chipset module contains the controller for the USB interface in IntelliStation Z Pro computers. (Refer to “Chip Set Control” on page 7 for information on the PIIX4 module.) Two USB ports are provided on the rear connector panel of the computers. A USB-enabled device can be attached to each port, and if that device is a hub, multiple peripheral devices can be attached to the hub and be used by the system. Plug and Play technology is used to recognize installed devices. The USB port functions at speeds of up to 1.5 Mbits per second or 12 Mbits per second. Data is transferred in either asynchronous or synchronous mode. The system does not support a keyboard attached to either of the USB ports as a boot device.

The USB is compliant with *Universal Host Controller Interface Design Guide 1.0*. Features provided by USB technology include:

- Support for up to 127 physical devices
- Connections of up to five meters in length from host to hub or hub to hub
- Support for hot pluggable devices
- Support for concurrent operation of multiple devices
- Support for different device bandwidths
- Guaranteed bandwidth and low latencies appropriate for telephony, audio, etc.

- Wide range of packet sizes
- Eight-signal USB cable

The external interface for the USB ports consists of two, 4-pin connectors. For information on connector pin assignments, see “USB Connectors” on page 45.

Super Input/Output Controller

Control of the integrated input/output (I/O) ports, diskette drive, and real-time clock is provided by the National Semiconductor PC97307 chip. This chip, which is compatible with *Plug and Play ISA Specification 1.0a*, supports and implements the following features:

- Diskette interface
- Parallel port
- Serial ports
- Keyboard and mouse ports
- General-purpose I/O ports
- Real-time clock

Diskette Interface

IntelliStation Z Pro computers support a maximum of two diskette drives and one tape backup drive. (Refer to “Internal Drives” on page 21 for more information.) The following is a list of devices that the diskette interface will support:

- 1.44 MB, 3.5-inch diskette drive
- 1.44 MB, 3.5-inch, 3-mode drive for Japan
- 5.25-inch, 1.2 MB diskette drive
- 1 Mbps, 500 Kbps, or 250 Kbps internal tape drive

Note: A 2.88 MB, 3.5-inch diskette drive is not supported.

The following table shows the typical system resource assignments for the diskette interface.

Table 2. System Resource Assignments for the Diskette Interface

Resource	Resource Assignment
ROM	None
RAM	None
I/O Address (Hex)	03F0–03F5 (diskette channel 0) 03F7, bit 7 (diskette change)
IRQ	6
DMA	2

When the computer is started, the resource assignments are subject to change during POST.

One shrouded, 34-pin, berg-strip connector is provided on the system board for the diskette drive. For information on connector pin assignments, see “Diskette Drive Connector” on page 39.

Parallel Port

One parallel port is integrated into the system board. Support for extended capabilities port (ECP), enhanced parallel port (EPP), and standard parallel port (SPP) modes is provided. These modes are selected through the Configuration/Setup Utility program, with the default mode set to SPP. The ECP and EPP modes are compliant with IEEE 1284.

The following table shows the typical system resource assignments for the parallel port.

Table 3. System Resource Assignments for the Parallel Port

Configuration	ROM	RAM	I/O Address (Hex)	IRQ	DMA
LPT1	None	None	03BC–03BE	7	3[2]
LPT2	None	None	0378-037F	7	3[2]
LPT3	None	None	0278-027F	5	3[2]

Note: The default setting for the parallel port is LPT1. When the computer is started, the resource assignments are subject to change during POST.

The external interface for the parallel port is a 25-pin, female, D-shell connector. For information on connector pin assignments, see “Parallel Port Connector” on page 45.

Serial Ports

The serial port subsystem consists of two universal asynchronous receiver/transmitters (UARTs) that are PC16550A- and NS16450-compatible. The serial ports include a 16-byte data first-in first-out (FIFO) buffer and have programmable baud rate generators. The UARTs function independently of one another, and both can be used in normal mode, which is inclusive of modem control circuitry. UART2 function is determined at boot time via the Configuration/Setup Utility program and can only be altered by changing setup and rebooting the computer.

The following table shows the typical system resource assignments for the serial ports.

Table 4. System Resource Assignments for the Serial Ports

Configuration	ROM	RAM	I/O Address (Hex)	IRQ	DMA
COM1	None	None	03F8-03FF	4	None
COM2	None	None	02F8-02FF	3	None
COM3	None	None	03E8-03EF	4	None
COM4	None	None	02E8-02EF	3	None

The default setting for serial port 1 is COM1. For serial port 2, the default setting is COM2. When the computer is started, the resource assignments are subject to change during POST.

The external interface for the serial ports consists of two, 9-pin, male, D-shell connectors. For information on connector pin assignments, see “Serial Port Connectors” on page 46.

[2] ECP/EPP mode only.

Keyboard and Mouse Ports

The keyboard-and-mouse subsystem is controlled by a general purpose, 8-bit microcontroller. The controller consists of 256 bytes of data memory and 2 KB of read-only memory (ROM).

The controller has two logical devices; one controls the keyboard, and the other controls the mouse. The keyboard has two fixed I/O addresses and a fixed IRQ line (IRQ1). The keyboard can operate without a companion mouse, but the mouse can only operate with its companion keyboard. The mouse has a fixed IRQ line (IRQ12), but it does not have its own I/O address; it relies on the addresses used by the keyboard.

The following table shows the typical system resource assignments for the keyboard and mouse.

Table 5. System Resource Assignments for the Keyboard and Mouse

Configuration	ROM	RAM	I/O Address (Hex)	IRQ	DMA
Keyboard and mouse	None	None	0060, 0064	1 (keyboard) 12 (mouse)	None
Keyboard only	None	None	0060, 0064	1	None

Note: Keyboard and mouse is the default.

When the computer is started, the resource assignments are subject to change during POST.

For an external interface, the keyboard and mouse each have a 6-pin connector. For information on connector pin assignments, see “Keyboard and Mouse Port Connectors” on page 46.

Real-Time Clock

The low-power, real-time clock provides a time-of-day clock and a calendar. The clock is accurate to +/– 12 minutes per year. The clock settings are maintained by an external battery source at +2.4 volts. The life expectancy of the battery is approximately 2.25 years.

An external crystal is used to drive the real-time clock, and the battery is used to maintain the state of the CMOS RAM when the power to the computer is turned off. (The system has 242 bytes of battery-backed CMOS RAM in two banks.) If the CMOS RAM becomes corrupted and the system will not boot, a jumper is included on the system board to clear CMOS RAM so that POST can set CMOS RAM to factory default values.

The following table shows the typical system resource assignments for the real-time clock.

Table 6. System Resource Assignments for the Real-Time Clock

Resource	Resource Assignment
ROM	None
RAM	None
I/O Address (Hex)	0070, bits 6—0 (address) 0071 (data) 0072—0077 (address and data)
IRQ	8
DMA	None

When the computer is started, the resource assignments are subject to change during POST.

Video Subsystem

A high-performance, high-resolution graphics adapter provides the video subsystem and monitor connection for IntelliStation Z Pro (Type 6865) computers. The type of graphics adapter installed varies with computer model. One of the following is preinstalled in an expansion slot:

- A Matrox AGP graphics adapter.
- An Intergraph PCI graphics adapter

The monitor connector is located on the graphics adapter.

- The Intergraph PCI graphics adapter is a high-performance graphics adapter with a graphics engine, a texture engine, a 16 MB frame buffer, and 16 MB of texture memory. It also provides an expansion connector to attach an optional geometry accelerator PCI adapter for further performance enhancement. It has two external connectors.
  - The round, 5-pin connector is a stereo sync output jack. This jack provides a connection to the emitter module of a pair of LCD shutter glasses.
  - The blue, 15-pin connector is a monitor port.
- The Matrox AGP adapter is a high-performance, 2D graphics adapter with 8 MB of memory. It has a blue, 15-pin monitor connector and an upgrade connector for multimedia options (MPEG decoding and encoding, video in and out, and TV tuner).

Video Device Drivers

Video device drivers for the graphics adapter are provided on the *Ready-to-Configure Utility Program CD* that comes with IntelliStation Z Pro computers. Instructions for installing the device drivers are provided on the *Ready-to-Configure Utility Program CD* in README files that correspond to the operating system being used.

Video device drivers have already been installed in computers that come with IBM-preinstalled software.

Audio Subsystem

IntelliStation Z Pro (Type 6865) computers have an integrated Crystal 4235 audio subsystem that supports SoundBlaster and Microsoft Windows Sound System applications. Three audio ports are also provided. These features provide the ability to play back and capture sound and music, enabling the user to enjoy sound with multimedia applications.

The integrated audio controller provides the following:

- ISA bus interface
- 16-bit codec/mixer

The audio ports in IntelliStation Z Pro (Type 6865) computers are industry-standard, 3.5 mm (1/8") mini-jacks and are located on the rear connector panel of the computer. A description of the audio ports follows.

- Audio Line Out: This jack, which is located on the rear connector panel, is used to send audio signals from the computer to external devices, such as headphones, stereo-powered speakers with built-in amplifiers, multimedia keyboards, or the Audio Line In jack on a stereo system. In order to hear audio, one of these external devices must be connected to the Audio Line-Out port on the computer.
- Audio Line In: This jack is used to send audio signals from an external device (such as a CD player or stereo) to the computer so that the signals can be recorded on the hard disk. (However, the input level must be reduced accordingly using the mixer provided in the computer operating system.)
- Microphone: This jack is used to connect a microphone to the computer so that voice or other sounds can be recorded on the hard disk. This jack can also be used by speech-recognition software.

  Note: If interference or speaker feedback is experienced while recording, reducing the microphone recording volume (gain) might help to alleviate the problem.

The following table shows the system resource assignments for the audio controller.

Table 7. System Resource Assignments for the Audio Controller

Resource	Resource Assignment
ROM	None
RAM	None
I/O Address (Hex)	220-22F, 388-38B, 534-537
IRQ	5
DMA	1, 5

When the computer is started, the resource assignments are subject to change during POST.

Ethernet Subsystem

The system board contains an Intel 82558 Ethernet controller with Wake on LAN. This subsystem is a high-performance Ethernet LAN interface that provides both 10Base-T and 100Base-TX connectivity using a single RJ-45 connector. The Ethernet controller, which is a Plug and Play device and a PCI 2.1 Bus Master, features the following:

- IEEE 802.3 compliance, 10 and 100 Mbps
- Support for 10Base-T and 100Base-TX with PCI bus interface
- Viewable media access control (MAC) address
- 3 Kbyte transmit FIFO and 3 Kbyte receive FIFO
- Auto-negotiation
- Full duplex capability
- Full NOS support

The system board also includes a discrete Wake on LAN controller (MagPack). This controller can be disabled in the Configuration/Setup Utility program.

Note: For compliance with FCC Class A radiation limits, all Ethernet cabling attached to IntelliStation Z Pro computers must be Class 5, regardless of the speed (10 Mbit or 100 Mbit).

The following table shows the system resource assignments for the Ethernet controller.

Table 8. System Resource Assignments for the Ethernet Controller

Resource	Resource Assignment
ROM	None
RAM	None
I/O Address (Hex)	Plug and Play
IRQ	Plug and Play
DMA	None

When the computer is started, the resource assignments are assigned during POST.

The external interface for the Ethernet feature is an 8-pin, RJ-45 connector. For information on connector pin assignments, see “Ethernet Connector” on page 48.

Small Computer System Interface (SCSI)

IntelliStation Z Pro (Type 6865) computers have a preinstalled Adaptec 2940U2W SCSI PCI adapter that provides an interface through which the computer can communicate with SCSI-compatible devices, such as hard disk drives, CD-ROM drives, tape drives, read-and-write optical drives, scanners, and printers. The Adaptec 2940U2W SCSI PCI adapter has 4 connectors. Two of the connectors (one internal and one external) are for connecting Ultra2 SCSI devices. These are labelled *Ultra2-LVD/SE*. The other internal 68-pin connector is connecting Fast/Wide Ultra devices. The internal 50-pin connector is for connecting Fast/Ultra Narrow SCSI devices.

For further information on the SCSI interface, including instructions for installing and configuring SCSI devices, refer to the SCSI documentation provided on the *Ready-to-Configure Utility Program CD* that comes with IntelliStation Z Pro computers. Also refer to *Installing Options in Your IntelliStation Z Pro*.

System Management Controller

The system board contains a system management chip that monitors the computer at all times looking for potential hardware failures. This chip is programmed with predetermined threshold values for the following:

- System temperature
- Fan speed
- Power supply voltages (+5, +12, –12, +3.3, Vcore)
- Microprocessor voltages
- Intrusion detect for security (detects when chassis lid has been removed, even if power is off)

During system operation, Desktop Management Interface (DMI) code polls the chip and generates an alert if the measured value is outside of the programmed minimum and maximum range. The alert can be provided to a network administrator across a LAN.

Note: DMI is software used to gather information about the hardware and software in a computer. It allows network administrators to remotely monitor and control the computer. DMI can be used to remotely track many types of information about networked PCs. This information can be accessed using a DMI browser. DMI browsers are provided by all major operating system and all major LAN management packages.

The following table shows the typical system resource assignments for the system management controller.

Table 9. System Resource Assignments for the System Management Controller

Resource	Resource Assignment
ROM	None
RAM	None
I/O Address (Hex)	None
IRQ	None
DMA	None

When the computer is started, the resource assignments are subject to change during POST.

System Board Jumpers

Jumpers are provided on the system board to provide control over the following:

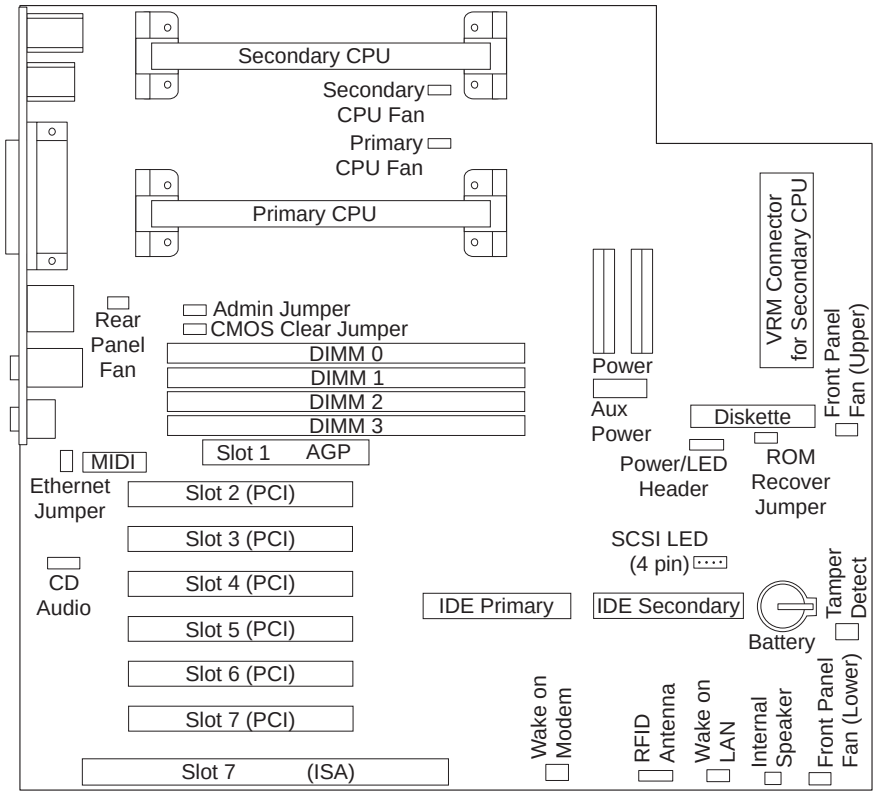
- Clear CMOS
- Enable/Disable Ethernet
- Erase Administrator Password
- ROM Recovery.

See “Physical Layout of System Board” on page 19 for the location of the jumpers.

Function	Jumper Pins
CMOS Jumper	
Normal CMOS Operation	1 - 2 (normal position)
Clear CMOS	2 - 3
Ethernet Jumper	
Enable Ethernet	1 - 2 (normal position)
Disable Ethernet	2 - 3
Admin Jumper	
Enable setting, changing, or deleting the adminstrator password protected by enhanced security	1 - 2
Disable setting, changing, or deleting the adminstrator password protected by enhanced security	2 - 3 (normal position)
ROM Recover Jumper (Boot Block)	
Normal ROM operation	1 - 2 (normal position)
ROM recovery mode	2 - 3

Physical Layout of System Board

The system board contains all the cable connectors for the system. The following illustration shows the physical layout of the system board. Also, a diagram of the board, including jumper settings, is attached inside the computer.



Adapters plug into the PCI, ISA, or AGP expansion connectors (slots) on the system board. There are six expansion slots: four dedicated PCI, one shared ISA/PCI, and one dedicated AGP. Signals from adapters are routed to the PCI, ISA, or AGP buses. Each PCI-expansion connector provides a 32-bit-wide data path. The ISA-expansion connector provides a 16-bit-wide data path, and the AGP connector provides a 32-bit wide data path. The shared ISA/PCI slot will accommodate either an ISA adapter installed in the ISA connector, or a PCI adapter installed into the PCI connector. The shared slot cannot accommodate ISA and PCI adapters at the same time.

Each PCI-expansion connector is capable of driving one, low-power Schottky load. The ISA-expansion connector is capable of driving two, low-power Schottky loads. The ISA bus is permanently set to the PCI bus speed divided by four.

The PCI bus shares interrupts with the ISA bus. Free interrupts are automatically assigned to PCI devices during POST. If no interrupts are available for the PCI devices, an 18xx POST error message is generated.

For information on connector pin assignments, see “PCI Bus Connectors” on page 34, “ISA Bus Connector” on page 32, and “AGP Bus Connector” on page 36.

Input/Output Connectors

The following diagram shows the connector panel and expansion slots located on the back side of the computer.

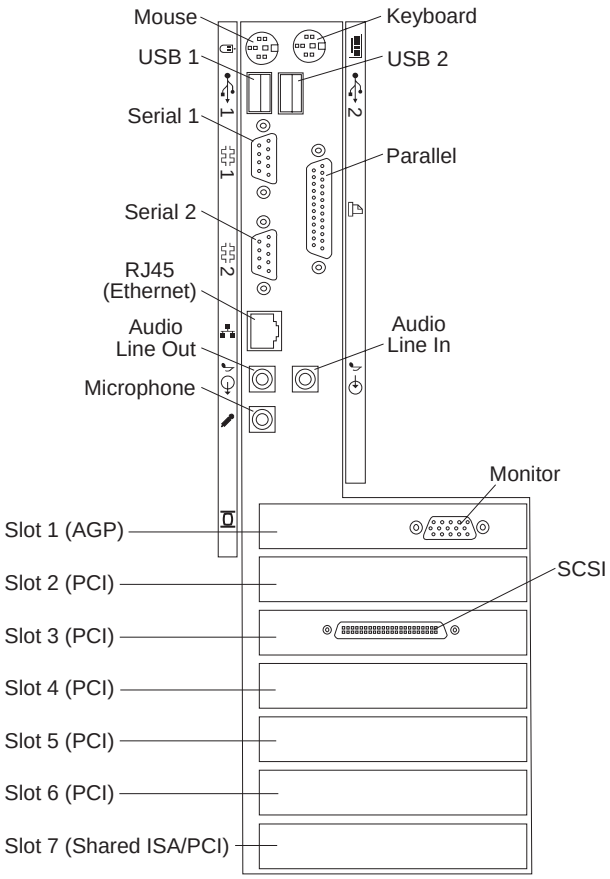


Figure 1. Rear Connector Panel and Expansion Slots

Chapter 3. Adapters and Internal Drives

This chapter provides information on adapters and internal drives supported by IntelliStation Z Pro computers.

Adapters

This section provides important information on adapter installation.

Note: IntelliStation Z Pro computers do not support IDE expansion adapters or the IBM PCMCIA adapter for PCI.

Wake on LAN Adapters

Wake on LAN adapters have two headers: a 3-pin, right-angle header for providing AUX5 (Auxiliary 5 volts), and a 2-pin straight header for connecting the wakeup signal to the system board. IntelliStation Z Pro computers have a 3-pin header that provides the AUX5 and wakeup signal connections. The Wake on LAN adapter option will provide a Y-cable that has the 3-pin connector on one end and splits into the 3-pin and 2-pin connectors required to interface the card. When a Wake on LAN adapter is installed in the system and attached to the AUX5 power, the system board Ethernet function must be disabled via switch 6 on the system board (refer to “System Board Jumpers” on page 18 for switch information).

Internal Drives

The diskette, IDE, and SCSI interfaces provide connectors for attaching internal drives.

IntelliStation Z Pro computers come standard with an internal diskette drive, an internal EIDE or SCSI hard disk drive, and an internal CD-ROM drive.

The following tables show the characteristics of internal drives that come standard with or are available for IntelliStation Z Pro computers.

Table 10. Diskette Drives

Characteristics	**Number/Size**
Standard	One 3.5-inch, 1.44 MB diskette drive
Maximum	Two diskette drives and one tape backup

Table 11. IDE and SCSI Devices

Characteristics	**Number/Size or Speed**
Standard	One EIDE or one Ultra Wide SCSI hard disk drive (size varies by model)
Standard	One IDE CD/ROM drive
Optional	IDE or SCSI hard disk drives and tape backup drives
Maximum IDE Devices	Four total
Maximum SCSI Devices	Refer to the SCSI documentation on the *Ready-to-Configure Utility Program CD* that comes with IntelliStation Z Pro (Type 6865) computers

Note: The actual number of internal devices that can be installed in IntelliStation Z Pro computers is limited by the number of available drive bays.

Chapter 4. Power Supply

Power requirements are supplied by a 330-watt power supply in the IntelliStation Z Pro. The power supply provides 3.3-volt power for the Pentium Xeon microprocessor and core chip sets, as well as 5-volt power for ISA and PCI adapters. Also included is an auxiliary 5-volt (AUX 5) supply to provide power to power management circuitry and the system board Ethernet function, or a Wake on LAN adapter.

The power supply converts ac input voltages into dc output voltages. The power supply operates at either 115 V ac or 230 V ac. The power supply automatically senses the ac input voltage so that no switch selection is required when installing the computer.

The power supply provides power for the following components:

- System board
- ISA and PCI adapters
- Internal drives
- Keyboard and auxiliary devices
- USB devices

A logic signal on the power connector controls the power supply. (The front panel switch is not directly connected to the power supply.)

The power supply connects to the system board with a 2 x 10 connector and a 1 x 6 connector.

Power Input

For power input specifications, refer to Table 25 on page 27.

Power Output

The following tables show the power supply capacity per voltage for the IntelliStation Z Pro. In the tables, amperes are designated with an *A*, and milliamperes with an *mA*.

Table 12. Power Output for 330-Watt Power Supply

Output Voltage	Minimum to Maximum	Regulation Limits
+5 V dc	1.5 to 32.0 A[3]	+5% to –4%
+12 V dc	0.2 to 8.5 A	+5% to –5%
–12 V dc	0.0 to 0.7 A	+10% to –9%
–5 V dc	0.0 to 0.4 A	+10% to –10%
+3.3 V dc	0.0 to 25.0 A[3]	±5%
+5 V dc (auxiliary)	5 mA to 0.75 A	±5%

The power supply provides separate voltage sources for the system board and internal storage devices. The following tables show the maximum power that specific system components can draw. In normal operation, components draw less current than the maximum shown.

Table 13. System Board Power Connectors

Supply Voltage	Maximum Current	Regulation Limits
+3.3 V dc	8520 mA	+5.0% to –5.0%
+5.0 V dc	2000 mA	+5.0% to –4.0%
+12.0 V dc	25.0 mA	+5.0% to –5.0%
–12.0 V dc	25.0 mA	+10.0% to –9.0%

Table 14. ISA-Bus Adapters

Supply Voltage	Maximum Current	Regulation Limits
+5.0 V dc	2000 mA	+5.0% to –4.0%
–5.0 V dc	100 mA	±10.0%
+12.0 V dc	175 mA	+5.0% to –5.0%
–12.0 V dc	100 mA	+10.0% to –9.0%

[3] Simultaneous loading of +3.3 V dc and +5 V dc must not exceed 217 watts.

Table 15. PCI-Bus Adapters (Per Slot)		
Supply Voltage	**Maximum Current**	**Regulation Limits**
+5.0 V dc	5000 mA	+5.0% to –4.0%
+3.3 V dc	7600 mA	+5.0% to –5.0%
+12 V dc	500 mA	±5.0%
–5.0 V dc	100 mA	±10.0%

Notes:

1. For each PCI connector, the maximum power consumption is rated at 25 watts for +5 V and +3.3 V combined.
2. Maximum current cannot be supplied to all components at all times. System power and cooling are designed to support the statistical RMS power load and typical combinations of adapters.

Table 16. AGP Adapter		
Supply Voltage	**Maximum Current**	**Regulation Limits**
+3.3 V dc	7600 mA	±10.0%

Table 17. Internal 9.11 GB SCSI Drive		
Supply Voltage	**Maximum Current**	**Regulation Limits**
+5.0 V dc	1085 mA (idle); 1133 mA (typical); 1300 (peak)	+5.0% to –5.0%
+12.0 V dc	850 mA (idle); 2050 mA (peak); 2711 mA (maximum)	+5.0% to –5.0%

Note: Some adapters and hard disk drives draw more current than the recommended limits. These adapters and drives can be installed in the system; however, the power supply will shut down if the total power used exceeds the maximum power that is available.

Table 18. Keyboard Port		
Supply Voltage	**Maximum Current**	**Regulation Limits**
+5.0 V dc	500 mA	+5.0% to –4.0%

Table 19. USB Port		
Supply Voltage	**Maximum Current**	**Regulation Limits**
+5.0 V dc	500 mA	+5.0% to –4.0%

Output Protection

The power supply protects against output overcurrent, overvoltage, and short circuits.

A short circuit that is placed on any dc output (between outputs or between an output and dc return) latches all dc outputs into a shutdown state, with no damage to the power supply. If this shutdown state occurs, the power supply returns to normal operation only after the fault has been removed and the ac input voltage has been turned off for at least five seconds.

If an overvoltage fault occurs (in the power supply), the power supply latches all dc outputs into a shutdown state before any output exceeds 130% of the nominal value of the power supply.

Power Connectors

The power supply connects to the system board via a 2 x 10 connector and a 1 x 6 connector.

The power supply provides 4-pin connectors for attaching internal devices. The IntelliStation Z Pro has two diskette and six DASD connectors. The following tables list the pin assignments for these connectors.

Note: The total power used by any of the following connectors must not exceed the amount shown in Table 17 on page 24.

Table 20. Pin Assignments for the 4-Pin Power Connectors

Connector	Location	Pin 1	Pin 2	Pin 3	Pin 4
P3	3.5-inch diskette drive	+5 V	Ground	Ground	+12 V
P5/P6, P7, P8/P9, P10	DASD	+12 V	Ground	Ground	+5 V

Chapter 5. Physical Specifications

The tables in this chapter list the physical specifications for IntelliStation Z Pro computers.

Note: The computers are electromagnetically compatible with FCC Class A.

Table 21. Size

Description	Measurement
Depth	460 mm (18.1 in.)
Height	492 mm (19.4 in.)
Width	200 mm (7.9 in.)

Table 22. Weight

Description	Measurement
Maximum configuration (as shipped)[4]	20.5 kg (45 lb)

In the following table, the maximum altitude at which the specified air temperatures apply is 2134 m (7000 ft). At higher altitudes, the maximum air temperatures are lower than those specified.

Table 23. Air Temperature

Description	Measurement
System on	10 to 32°C (50 to 95°F)
System off	-40 to 70°C (-40 to 158°F)

Table 24. Humidity

Description	Measurement
System on	8% to 80%
System off	8% to 80%

[4] Maximum configuration weight depends on options installed. The weight given here is for a computer fully populated with options.

Power consumption and heat output vary depending on the number and type of optional features installed and the power-management optional features in use. In the following two tables, maximum power and heat specifications are based on the maximum capacity of the power supply.

Table 25. Electrical Input

Description	Measurement
Low range	100 V ac (minimum) 127 V ac (maximum) Current rating: 5.0 amps
High range	200 V ac (minimum) 240 V ac (maximum) Current rating: 3.0 amps
Sine-wave input	50 to 60 Hz is required
Input kilovolt-amperes, approximate maximum (as shipped)	0.75 kVA

Table 26. Heat Output (Approximate)

Description	Measurement
Maximum configuration (as shipped)	106 W (361 Btu per hour)
Theoretical maximum configuration[5]	460 W (1564 Btu per hour)

The levels in the following table were measured in controlled acoustical environments according to procedures specified by the American National Standards Institute (ANSI) S12.10 and ISO 7779, and are reported in accordance with ISO 9296. Actual sound pressure levels in your location might exceed the average values stated because of room reflections and other nearby noise sources. The declared sound power levels indicate an upper limit, below which a large number of computers will operate.

Table 27. Acoustical Noise Emission Values

Description	Measurement
Average sound pressure levels (operator position)	44 dB operating 40 dB idle
Average sound pressure levels (bystander position of 3.3 ft)	40 dB operating 37 dB idle
Declared (upper limit) sound power levels	5.5 bels operating 5.2 bels idle

The airflow rating for IntelliStation Z Pro (Type 6865) computers is approximately 0.92 cubic meters/minute (32.5 CFM).

[5] Under typical maximum configurations, the heat output will be significantly below the theoretical maximum.

Chapter 6. System Compatibility

This chapter provides information on some of the hardware, software, and BIOS compatibility issues for the IntelliStation Z Pro computers (Type 6865). For a list of compatible hardware and software option packages available, refer to the *Compatibility Report* for these computers on the World Wide Web at http://www.pc.ibm.com/us/intellistation/tech_library.html.

Hardware Compatibility

This section discusses hardware and BIOS compatibility issues that must be considered when designing application programs.

Many of the interfaces are the same as those used by the IBM Personal Computer AT. In most cases, the command and status organization of these interfaces is maintained.

The functional interfaces are compatible with the following interfaces:

- The Intel 8259 interrupt controllers (edge-triggered mode)
- The National Semiconductor NS16450 and NS16550A serial communication controllers
- The Motorola MC146818 Time of Day Clock command and status (CMOS reorganized)
- The Intel 8254 timer, driven from a 1.193 MHz clock (channels 0, 1, and 2)
- The Intel 8237 DMA controller, except for the Command and Request registers and the Rotate and Mask functions; the Mode register is partially supported
- The Intel 8272 or 82077 diskette drive controllers
- The Intel 8042 keyboard controller at addresses 0060h and 0064h
- All video standards using VGA, EGA, CGA, MDA, and Hercules modes
- The parallel printer ports (Parallel 1, Parallel 2, and Parallel 3) in compatibility mode

Use the following information to develop application programs. Whenever possible, use the BIOS as an interface to hardware to provide maximum compatibility and portability of applications among systems.

Hardware Interrupts

Hardware interrupts are level-sensitive for PCI interrupts and edge-sensitive for ISA interrupts. The interrupt controller clears its in-service register bit when the interrupt routine sends an End of Interrupt (EOI) command to the controller. The EOI command is sent regardless of whether the incoming interrupt request to the controller is active or inactive.

The interrupt-in-progress latch is readable at an I/O-address bit position. This latch is read during the interrupt service routine and might be reset by the read operation, or it might require an explicit reset.

Note: For performance and latency considerations, designers might want to limit the number of devices sharing an interrupt level.

With level-sensitive interrupts, the interrupt controller requires that the interrupt request be inactive at the time the EOI command is sent; otherwise, a new interrupt request will be detected. To avoid this, a level-sensitive interrupt handler must clear the interrupt condition (usually by a read or write operation to an I/O port on the device causing the interrupt). After processing the interrupt, the interrupt handler:

1. Clears the interrupt
2. Waits one I/O delay
3. Sends the EOI
4. Waits one I/O delay
5. Enables the interrupt through the Set Interrupt Enable Flag command

Hardware interrupt IRQ9 is defined as the replacement interrupt level for the cascade level IRQ2. Program interrupt sharing is implemented on IRQ2, interrupt 0Ah. The following processing occurs to maintain compatibility with the IRQ2 used by IBM Personal Computer products:

1. A device drives the interrupt request active on IRQ2 of the channel.
2. This interrupt request is mapped in hardware to IRQ9 input on the second interrupt controller.
3. When the interrupt occurs, the system microprocessor passes control to the IRQ9 (interrupt 71h) interrupt handler.
4. This interrupt handler performs an EOI command to the second interrupt controller and passes control to the IRQ2 (interrupt 0Ah) interrupt handler.
5. This IRQ2 interrupt handler, when handling the interrupt, causes the device to reset the interrupt request before performing an EOI command to the master interrupt controller that finishes servicing the IRQ2 request.

APIC Controller

IntelliStation Z Pro computers provide an Advanced Programmable Interrupt Controller (APIC) to enable multi-processing and to allow advanced interrupt handling in uni-processor configurations. The APIC architecture consists of local APIC(s) inside of each microprocessor and a single IO APIC to distribute interrupts to the microprocessors. Interrupts are handled as a default by legacy 8259 devices inside the PIIX4 controller. The APIC resources, when utilized by the operating system, essentially replace the legacy 8259 controllers and provide advanced capability.

The APIC resources are made available to the operating system via a software table. The following table details the hardware connections on the system board that are relevant.

Table 28. IO APIC Resources

IO APIC Input	Bus Connection	Notes[6]
INT0	INTR	8259 Output
INT1	IRQ 1	Legacy Connection - Keyboard
INT2	IRQ 0	Legacy Connection - Timer
INT3	IRQ 3	Legacy Connection - COM 2
INT4	IRQ 4	Legacy Connection - COM 1
INT5	IRQ 5	Legacy Connection - LPT3
INT6	IRQ 6	Legacy Connection - Diskette
INT7	IRQ 7	Legacy Connection - LPT1/LPT2
INT8	IRQ 8	Legacy Connection - RTC
INT9	IRQ 9	Legacy Connection
INT10	IRQ 10	Legacy Connection
INT11	IRQ 11	Legacy Connection
INT12	IRQ 12	Legacy Connection - Mouse
INT13	IRQ 13	Legacy Connection - Math coprocessor
INT14	IRQ 14	Legacy Connection - IDE primary
INT15	IRQ 15	Legacy Connection - IDE secondary
INT16	PCI INT 1	IOAPIC mode only
INT17	PCI INT 2	IOAPIC mode only
INT18	PCI INT 3	IOAPIC mode only
INT19	PCI INT 4	IOAPIC mode only
INT20	SCSI - Internal	IOAPIC mode only
INT22	System Management Controller	IOAPIC mode only
INT23	SMI	IOAPIC mode only

Diskette Drives and Controller

The following table shows the reading, writing, and formatting capabilities for the diskette drive type supported by IntelliStation Z Pro computers.

Table 29. 3.5-Inch Diskette Drive Reading, Writing, and Formatting Capabilities

Diskette Drive Type	720 KB Mode	1.44 MB Mode	2.88 MB Mode
1.44 MB drive	RWF	RWF	Not supported

[6] Connections noted here are typical only, and may be modified by software control.

Copy Protection

The following methods of copy protection might not work in systems using the 3.5-inch, 1.44 MB diskette drive.

- Bypassing BIOS routines:
  - Data transfer rate: BIOS selects the proper data transfer rate for the media being used.
  - Diskette parameter table: Copy protection, which creates its own diskette parameter table, might not work in these drives.
- Diskette drive controls:
  - Rotational speed: The time between two events in a diskette drive is a function of the controller.
  - Access time: Diskette BIOS routines must set the track-to-track access time for the different types of media that are used in the drives.
  - 'Diskette change' signal: Copy protection might not be able to reset this signal.
- Write-current control: Copy protection that uses write-current control does not work, because the controller selects the proper write current for the media that is being used.

Hard Disk Drives and Controller

Reading from and writing to the hard disk is initiated in the same way as in other IBM Personal Computer products; however, new functions are supported.

Software Compatibility

To maintain software compatibility, the interrupt polling mechanism that is used by IBM Personal Computer products is retained. Software that interfaces with the reset port for the IBM Personal Computer positive-edge interrupt sharing (hex address 02F*x* or 06F*x*, where *x* is the interrupt level) does not create interference.

Software Interrupts

With the advent of software interrupt sharing, software interrupt routines must daisy-chain interrupts. Each routine must check the function value, and if it is not in the range of function calls for that routine, it must transfer control to the next routine in the chain. Because software interrupts are initially pointed to address 0:0 before daisy chaining, check for this case. If the next routine is pointed to address 0:0 and the function call is out of range, the appropriate action is to set the carry flag and do a RET 2 to indicate an error condition.

Machine-Sensitive Programs

Programs can select machine-specific features, but they must first identify the machine and model type. IBM has defined methods for uniquely determining the specific machine type. The machine model byte can be found through Interrupt 15H, Return System Configuration Parameters function ((AH)=C0H).

Appendix A. Connector Pin Assignments

The following tables show the pin assignments for various system board connectors.

ISA Bus Connector

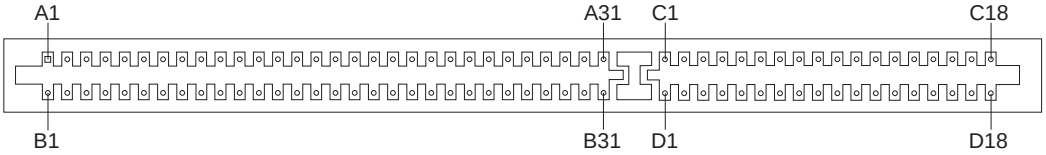


Figure 2. ISA Bus Connector

The ISA bus connector is located on the system board.

Table 30 (Page 1 of 2). Pin Assignments for the ISA Bus Connectors

Pin	Signal Name	I/O	Pin	Signal Name	I/O
B1	Ground	NA	A1	IOCHCK#	I
B2	RESET DRV	O	A2	SD7	I/O
B3	+5 V dc	NA	A3	SD6	I/O
B4	IRQ2/9	I	A4	SD5	I/O
B5	–5 V dc	NA	A5	SD4	I/O
B6	DRQ2	I	A6	SD3	I/O
B7	–12 V dc	NA	A7	SD2	I/O
B8	0WS#	I	A8	SD1	I/O
B9	+12 V dc	NA	A9	SD0	I/O
B10	Ground	NA	A10	IOCHRDY	I
B11	SMEMW#	O	A11	AEN	O
B12	SMEMR#	O	A12	SA19	I/O
B13	IOW#	I/O	A13	SA18	I/O
B14	IOR#	I/O	A14	SA17	I/O
B15	DACK3#	O	A15	SA16	I/O
B16	DRQ3	I	A16	SA15	I/O
B17	DACK1#	O	A17	SA14	I/O
B18	DRQ1	I	A18	SA13	I/O
B19	REFRESH#	I/O	A19	SA12	I/O
B20	CLK	O	A20	SA11	I/O
B21	IRQ7	I	A21	SA10	I/O
B22	IRQ6	I	A22	SA9	I/O
B23	IRQ5	I	A23	SA8	I/O
B24	IRQ4	I	A24	SA7	I/O
B25	IRQ3	I	A25	SA6	I/O
B26	DACK2#	O	A26	SA5	I/O
B27	TC	O	A27	SA4	I/O
B28	BALE	O	A28	SA3	I/O

Table 30 (Page 2 of 2). Pin Assignments for the ISA Bus Connectors

Pin	Signal Name	I/O	Pin	Signal Name	I/O
B29	+5 V dc	NA	A29	SA2	I/O
B30	OSC	O	A30	SA1	I/O
B31	Ground	NA	A31	SA0	I/O
D1	MEMCS16#	I	C1	SBHE#	I/O
D2	IOCS16#	I	C2	LA23	I/O
D3	IRQ10	I	C3	LA22	I/O
D4	IRQ11	I	C4	LA21	I/O
D5	IRQ12	I	C5	LA20	I/O
D6	IRQ15	I	C6	LA19	I/O
D7	IRQ14	I	C7	LA18	I/O
D8	DACK0#	O	C8	LA17	I/O
D9	DRQ0	I	C9	MEMR#	I/O
D10	DACK5#	O	C10	MEMW#	I/O
D11	DRQ5	I	C11	SD8	I/O
D12	DACK6#	O	C12	SD9	I/O
D13	DRQ6	I	C13	SD10	I/O
D14	DACK7#	O	C14	SD11	I/O
D15	DRQ7	I	C15	SD12	I/O
D16	+5 V dc	NA	C16	SD13	I/O
D17	MASTER#	I	C17	SD14	I/O
D18	Ground	NA	C18	SD15	I/O

PCI Bus Connectors

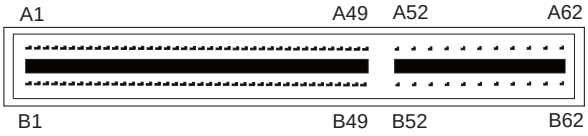


Figure 3. PCI Bus Connector

Note: The PCI bus connectors are located on the system board.

Table 31 (Page 1 of 2). Pin Assignments for the PCI Bus Connectors

Pin	Signal Name	I/O	Pin	Signal Name	I/O
A1	TRST#	O	B1	–12 V dc	NA
A2	+12 V dc	NA	B2	TCK	O
A3	TMS	O	B3	Ground	NA
A4	TDI	O	B4	TDO	I
A5	+5 V dc	NA	B5	+5 V dc	NA
A6	INTA#	I	B6	+5 V dc	NA
A7	INTC#	I	B7	INTB#	I
A8	+5 V dc	NA	B8	INTD#	I
A9	Reserved	NA	B9	PRSNT1#	I
A10	+5 V dc	NA	B10	Reserved	NA
A11	Reserved	NA	B11	PRSNT2#	I
A12	Ground	NA	B12	Ground	NA
A13	Ground	NA	B13	Ground	NA
A14	Reserved	NA	B14	Reserved	NA
A15	RST#	O	B15	Ground	NA
A16	+5 V dc	NA	B16	CLK	O
A17	GNT#	O	B17	Ground	NA
A18	Ground	NA	B18	REQ#	I
A19	Reserved	NA	B19	+5 V dc	NA
A20	Address/Data 30	I/O	B20	Address/Data 31	I/O
A21	+3.3 V dc	NA	B21	Address/Data 29	I/O
A22	Address/Data 28	I/O	B22	Ground	NA
A23	Address/Data 26	I/O	B23	Address/Data 27	I/O
A24	Ground	NA	B24	Address/Data 25	I/O
A25	Address/Data 24	I/O	B25	+3.3 V dc	NA
A26	IDSEL	O	B26	C/BE3#	I/O
A27	+3.3 V dc	NA	B27	Address/Data 23	I/O
A28	Address/Data 22	I/O	B28	Ground	NA
A29	Address/Data 20	I/O	B29	Address/Data 21	I/O
A30	Ground	NA	B30	Address/Data 19	I/O
A31	Address/Data 18	I/O	B31	+3.3 V dc	NA
A32	Address/Data 16	I/O	B32	Address/Data 17	I/O
A33	+3.3 V dc	NA	B33	C/BE2#	I/O
A34	FRAME#	I/O	B34	Ground	NA

Table 31 (Page 2 of 2). Pin Assignments for the PCI Bus Connectors

Pin	Signal Name	I/O	Pin	Signal Name	I/O
A35	Ground	NA	B35	IRDY#	I/O
A36	TRDY#	I/O	B36	+3.3 V dc	NA
A37	Ground	NA	B37	DEVSEL#	I/O
A38	STOP#	I/O	B38	Ground	NA
A39	+3.3 V dc	NA	B39	LOCK#	I/O
A40	SDONE	I/O	B40	PERR#	I/O
A41	SBO#	I/O	B41	+3.3 V dc	NA
A42	Ground	NA	B42	SERR#	I/O
A43	PCIPAR	NA	B43	+3.3 V dc	NA
A44	Address/Data 15	I/O	B44	C/BE1#	I/O
A45	+3.3 V	I/O	B45	Address/Data 14	I/O
A46	Address/Data 13	NA	B46	Ground	NA
A47	Address/Data 11	I/O	B47	Address/Data 12	I/O
A48	Ground	I/O	B48	Address/Data 10	I/O
A49	Address/Data 9	NA	B49	Ground	NA
A50	##Key##	NA	B50	##Key##	NA
A51	##Key##	NA	B51	##Key##	NA
A52	C/BE0#	I/O	B52	Address/Data 8	I/O
A53	+3.3 V dc	I/O	B53	Address/Data 7	I/O
A54	Address/Data 6	NA	B54	+3.3 V dc	NA
A55	Address/Data 4	I/O	B55	Address/Data 5	I/O
A56	Ground	I/O	B56	Address/Data 3	I/O
A57	Address/Data 2	NA	B57	Ground	NA
A58	Address/Data 0	I/O	B58	Address/Data 1	I/O
A59	+5 V dc	NA	B59	+5 V dc	NA
A60	REQ64#	I/O	B60	ACK64#	I/O
A61	+5 V dc	NA	B61	+5 V dc	NA
A62	+5 V dc	NA	B62	+5 V dc	NA

AGP Bus Connector

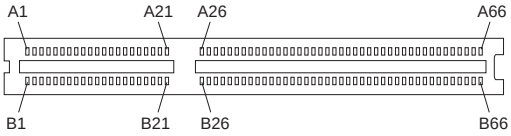


Figure 4. AGP Bus Connector

Note: The AGP bus connector is located on the system board.

Table 32 (Page 1 of 2). Pin Assignments for the AGP Bus Connector

Pin	Signal Name	Pin	Signal Name
A1	+12 V dc	B1	spare
A2	spare	B2	+5 V dc
A3	Reserved *	B3	+5 V dc
A4	USB-	B4	USB+
A5	Ground	B5	Ground
A6	INTA#	B6	INTB#
A7	RST#	B7	CLK
A8	GNT#	B8	REQ#
A9	VCC 3.3	B9	VCC 3.3
A10	ST1	B10	ST0
A11	Reserved	B11	ST2
A12	PIPE#	B12	RBF#
A13	Ground	B13	Ground
A14	Spare	B14	Spare
A15	SBA1	B15	SBA0
A16	VCC 3.3	B16	VCC 3.3
A17	SBA3	B17	SBA2
A18	Reserved	B18	SB_STB
A19	Ground	B19	Ground
A20	SBA5	B20	SBA4
A21	SBA7	B21	SBA6
A22	Key	B22	Key
A23	Key	B23	Key
A24	Key	B24	Key
A25	Key	B25	Key
A26	AD30	B26	AD31
A27	AD28	B27	AD29
A28	VCC 3.3	B28	VCC 3.3
A29	AD26	B29	AD27
A30	AD24	B30	AD25
A31	Ground	B31	Ground
A32	Reserved	B32	AD STB1
A33	C/BE3#	B33	AD23

Table 32 (Page 2 of 2). Pin Assignments for the AGP Bus Connector

Pin	Signal Name	Pin	Signal Name
A34	Vddq 3.3	B34	Vddq 3.3
A35	AD22	B35	AD21
A36	AD20	B36	AD19
A37	Ground	B37	Ground
A38	AD18	B38	AD17
A39	AD16	B39	C/BE2#
A40	Vddq 3.3	B40	Vddq 3.3
A41	FRAME#	B41	IRDY#
A42	Spare	B42	Spare
A43	Ground	B43	Ground
A44	Spare	B44	Spare
A45	VCC 3.3	B45	VCC 3.3
A46	TRDY#	B46	DEVSEL#
A47	STOP#	B47	Vddq 3.3
A48	Spare	B48	PERR#
A49	Ground	B49	Ground
A50	PAR	B50	SERR#
A51	AD15	B51	C/BE1#
A52	Vddq 3.3	B52	Vddq 3.3
A53	AD13	B53	AD14
A54	AD11	B54	AD12
A55	Ground	B55	Ground
A56	AD9	B56	AD10
A57	C/BE0#	B57	AD8
A58	Vddq 3.3	B58	Vddq 3.3
A59	Reserved	B59	AD STB0
A60	AD6	B60	AD7
A61	Ground	B61	Ground
A62	AD4	B62	AD5
A63	AD2	B63	AD3
A64	Vddq 3.3	B64	Vddq 3.3
A65	AD0	B65	AD1
A66	SMB1	B66	SMB0

* This reserved pin should be connected to Ground.

IDE Connectors

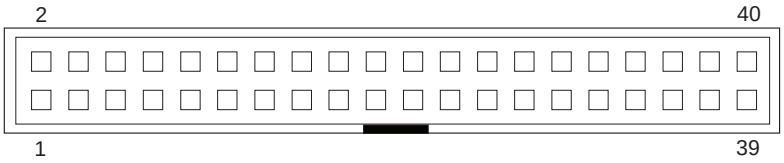


Figure 5. IDE Connector

The IDE connectors are 40-pin, shrouded berg strips located on the system board.

Table 33. Pin Assignments for the IDE Connectors

Pin	Signal Name	I/O	Pin	Signal Name	I/O
1	Reset	O	2	Ground	NA
3	D7	I/O	4	D8	I/O
5	D6	I/O	6	D9	I/O
7	D5	I/O	8	D10	I/O
9	D4	I/O	10	D11	I/O
11	D3	I/O	12	D12	I/O
13	D2	I/O	14	D13	I/O
15	D1	I/O	16	D14	I/O
17	D0	I/O	18	D15	I/O
19	Ground	NA	20	Key	NA
21	DMA REQ	NA	22	Ground	NA
23	IOW#	O	24	Ground	NA
25	IOR#	O	26	Ground	NA
27	IOCHRDY	I	28	CSEL	O
29	DMA ACK#	NA	30	Ground	NA
31	IRQ	I	32	CS16#	I
33	SA1	O	34	No connect	I
35	SA0	O	36	SA2	O
37	CS0#	O	38	CS1#	O
39	Active#	I	40	Ground	NA

Diskette Drive Connector

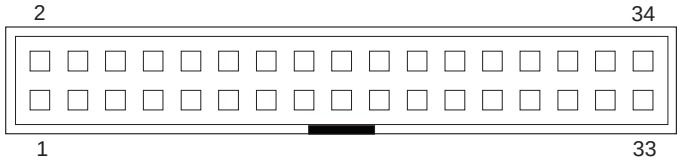


Figure 6. Diskette Drive Connector

The diskette drive connector is a 34-pin, shrouded berg strip located on the system board.

Table 34. Pin Assignments for the Diskette Drive Connector

Pin	Signal Name	I/O	Pin	Signal Name	I/O
1	Drive 2 installed#	I	2	High density select	O
3	Not connected	NA	4	Not connected	NA
5	Ground	NA	6	Data rate 0	NA
7	Ground	NA	8	Index#	I
9	Reserved	NA	10	Motor enable 0#	O
11	Ground	NA	12	Drive select 1#	O
13	Ground	NA	14	Drive select 0#	O
15	Ground	NA	16	Motor enable 1#	O
17	MSEN1	I	18	Direction in#	O
19	Ground	NA	20	Step#	O
21	Ground	NA	22	Write data#	O
23	Ground	NA	24	Write enable#	O
25	Ground	NA	26	Track 0#	I
27	MSEN0	I	28	Write protect#	I
29	Ground	NA	30	Read data#	I
31	Ground	NA	32	Head 1 select#	O
33	Ground	NA	34	Diskette change#	I

SCSI 50-pin Connector

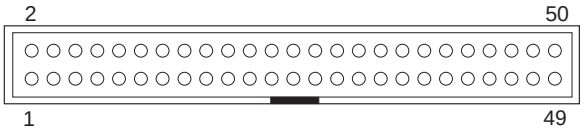


Figure 7. SCSI 50-pin Connector

This connector is a 50-pin, shrouded berg strip located on the system board.

Table 35. Pin Assignments for the SCSI 50-pin Connector

Pin	Signal Name	I/O	Pin	Signal Name	I/O
1	Ground	NA	2	DB0#	I/O
3	Ground	NA	4	DB1#	I/O
5	Ground	NA	6	DB2#	I/O
7	Ground	NA	8	DB3#	I/O
9	Ground	NA	10	DB4#	I/O
11	Ground	NA	12	DB5#	I/O
13	Ground	NA	14	DB6#	I/O
15	Ground	NA	16	DB7#	I/O
17	Ground	NA	18	DBP#	I/O
19	Ground	NA	20	Ground	NA
21	Ground	NA	22	Ground	I[7]
23	Ground	NA	24	Ground	NA
25	Not connected	NA	26	TERM PWR	NA
27	Ground	NA	28	Ground	NA
29	Ground	NA	30	Ground	NA
31	Ground	NA	32	ATN#	I/O
33	Ground	NA	34	Ground	NA
35	Ground	NA	36	BSY#	I/O
37	Ground	NA	38	ACK#	I/O
39	Ground	NA	40	RST#	I/O
41	Ground	NA	42	MSG#	I/O
43	Ground	NA	44	SEL#	I/O
45	Ground	NA	46	C/D#	I/O
47	Ground	NA	48	REQ#	I/O
49	Ground	NA	50	I/O#	I/O

[7] This pin is used to detect an attached cable.

SCSI 68-pin Connectors

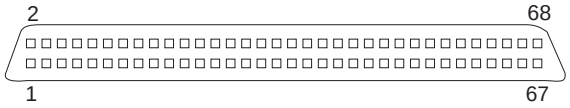


Figure 8. SCSI 68-pin Connector

These two connectors are 68-pin, shrouded berg strips located on the system board.

Table 36. Pin Assignments for the SCSI 68-pin Connector

Pin	Signal Name	I/O	Pin	Signal Name	I/O
1	Ground	NA	2	Ground	NA
3	Ground	NA	4	Ground	NA
5	Ground	NA	6	Ground	NA
7	Ground	NA	8	Ground	NA
9	Ground	NA	10	Ground	NA
11	Ground	NA	12	Ground	NA
13	Not connected	NA	14	Ground	NA
15	Ground	NA	16	Ground	NA
17	TERM PWR	NA	18	TERM PWR	NA
19	Reserved	NA	20	Ground	NA
21	Ground	NA	22	Ground	I
23	Ground	NA	24	Ground	NA
27	Ground	NA	28	Ground	NA
29	Ground	NA	30	Ground	NA
31	Ground	NA	32	Ground	NA
33	Ground	NA	34	Ground	NA
35	DB12#	I/O	36	DB13#	I/O
37	DB14#	I/O	38	DB15#	I/O
39	DBP1#	I/O	40	DB0#	I/O
41	DB1#	I/O	42	DB2#	I/O
43	DB3#	I/O	44	DB4#	I/O
45	DB5#	I/O	46	DB6#	I/O
47	DB7#	I/O	48	DBP#	I/O
49	Ground	NA	50	Ground	I[7]
51	TERM PWR	NA	52	TERM PWR	NA
53	Reserved	NA	54	Ground	NA
55	ATN#	I/O	56	Ground	NA
57	BSY#	I/O	58	ACK#	I/O
59	RST#	I/O	60	MSG#	I/O
61	SEL#	I/O	62	C/D#	I/O
63	REQ#	I/O	64	I/O#	I/O
65	DB8#	I/O	66	DB9#	I/O
67	DB10#	I/O	68	DB11#	I/O

System Memory Connectors

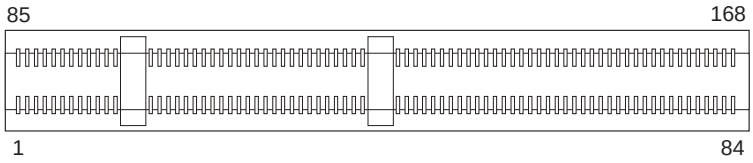


Figure 9. System Memory (DIMM) Connector

Each DIMM connector is a 168-pin, gold-lead, unbuffered, 3.3 V, SDRAM connector. These connectors are located on the system board.

Table 37 (Page 1 of 3). Pin Assignments for the DIMM Connectors

Pin	Signal Name	I/O	Pin	Signal Name	I/O
1	Ground	NA	85	Ground	NA
2	DQ0	I/O	86	DQ32	I/O
3	DQ1	I/O	87	DQ33	I/O
4	DQ2	I/O	88	DQ34	I/O
5	DQ3	I/O	89	DQ35	I/O
6	Vcc	I/O	90	Vcc	NA
7	DQ4	I/O	91	DQ36	NA
8	DQ5	I/O	92	DQ37	I/O
9	DQ6	I/O	93	DQ38	I/O
10	DQ7	I/O	94	DQ39	I/O
11	DQ8	I/O	95	DQ40	I/O
12	Ground	NA	96	Ground	NA
13	DQ9	I/O	97	DQ41	I/O
14	DQ10	I/O	98	DQ42	I/O
15	DQ11	O	99	DQ43	I/O
16	DQ12	O	100	DQ44	I/O
17	DQ13	O	101	DQ45	I/O
18	Vcc	O	102	Vcc	NA
19	DQ14	O	103	DQ46	I/O
20	DQ15	I/O	104	DQ47	I/O
21	CB0	I/O	105	CB4	I/O
22	CB1	I/O	106	CB5	I/O
23	Ground	I/O	107	Ground	NA
24	Not connected	NA	108	Not connected	NA
25	Not connected	NA	109	Not connected	NA
26	Vcc	I/O	110	Vcc	NA
27	/WE0	O	111	Not connected	NA
28	DQMB0	O	112	DQMB4	O
29	DQMB1	O	113	DQMB5	O
30	/S0	O	114	/S1	O
31	/OE0	O	115	Not connected	NA
32	Ground	O	116	Ground	NA

Table 37 (Page 2 of 3). Pin Assignments for the DIMM Connectors

Pin	Signal Name	I/O	Pin	Signal Name	I/O
33	A0	O	117	A1	O
34	A2	O	118	A3	O
35	A4	O	119	A5	O
36	A6	O	120	A7	O
37	A8	O	121	A9	O
38	A10	O	122	A11	O
39	Not connected	O	123	Not connected	O
40	Vcc	NA	124	Vcc	NA
41	Vcc	NA	125	Not connected	NA
42	Not connected	NA	126	Not connected	NA
43	Ground	NA	127	Ground	NA
44	/OE2	O	128	Not connected	NA
45	/S2	O	129	/S3	O
46	DQMB2	O	130	DQMB6	O
47	DQMB3	O	131	DQMB7	O
48	/WE2	O	132	Not connected	NA
49	Vcc	O	133	Vcc	NA
50	Not connected	NA	134	Not connected	NA
51	Not connected	NA	135	Not connected	NA
52	CB2	I/O	136	CB6	I/O
53	CB3	I/O	137	CB7	I/O
54	Ground	NA	138	Ground	NA
55	DQ16	I/O	139	DQ48	I/O
56	DQ17	I/O	140	DQ49	I/O
57	DQ18	I/O	141	DQ50	I/O
58	DQ19	I/O	142	DQ51	I/O
59	Vcc	NA	143	Vcc	NA
60	DQ20	I/O	144	DQ52	I/O
61	Not connected	NA	145	Not connected	NA
62	Not connected	NA	146	Not connected	NA
63	Not connected	NA	147	Pull Up	O
64	Ground	NA	148	Ground	NA
65	DQ21	I/O	149	DQ53	I/O
66	DQ22	I/O	150	DQ54	I/O
67	DQ23	I/O	151	DQ55	I/O
68	Ground	NA	152	Ground	NA
69	DQ24	I/O	153	DQ56	I/O
70	DQ25	I/O	154	DQ57	I/O
71	DQ26	I/O	155	DQ58	I/O
72	DQ27	I/O	156	DQ59	I/O
73	Vcc	NA	157	Vcc	NA
74	DQ28	I/O	158	DQ60	I/O
75	DQ29	I/O	159	DQ61	I/O

Table 37 (Page 3 of 3). Pin Assignments for the DIMM Connectors

Pin	Signal Name	I/O	Pin	Signal Name	I/O
76	DQ30	I/O	160	DQ62	I/O
77	DQ31	I/O	161	DQ63	I/O
78	Ground	NA	162	Ground	NA
79	Not connected	I/O	163	Not connected	NA
80	Not connected	I/O	164	Not connected	NA
81	Not connected	I/O	165	SA0	I/O
82	SDA	I/O	166	SA1	I/O
83	SCL	I/O	167	SA2	I/O
84	Vcc	NA	168	Vcc	I/O

Note: DU = Don't use

USB Connectors

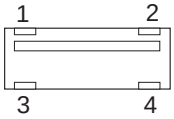


Figure 10. USB Connector

The external interface for the USB ports consists of two, 4-pin connectors.

Table 38. Pin Assignments for the USB Connectors

Pin	Signal Name	I/O
1	VCC	NA
2	-Data	I/O
3	+Data	I/O
4	Ground	NA

Parallel Port Connector

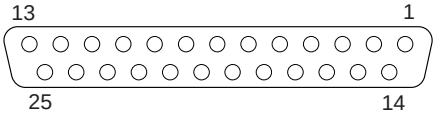


Figure 11. Parallel Port Connector

The external interface for the parallel port is a 25-pin, female, D-shell connector.

Table 39. Pin Assignments for the Parallel Port Connector

Pin	Signal Name	I/O	Pin	Signal Name	I/O
1	STROBE#	I/O	2	D0	I/O
3	D1	I/O	4	D2	I/O
5	D3	I/O	6	D4	I/O
7	D5	I/O	8	D6	I/O
9	D7	I/O	10	ACK#	I
11	BUSY	I	12	PE	I
13	SLCT	I	14	AUTO FD XT#	O
15	ERROR#	I	16	INIT#	O
17	SLCT IN#	O	18	Ground	NA
19	Ground	NA	20	Ground	NA
21	Ground	NA	22	Ground	NA
23	Ground	NA	24	Ground	NA
25	Ground	NA			

Serial Port Connectors

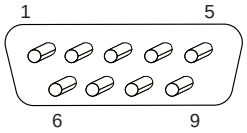


Figure 12. Serial Port Connector

The external interface for the serial ports consists of two, 9-pin, male, D-shell connectors.

Table 40. Pin Assignments for the Serial Port Connectors

Pin	Signal Name	I/O	Pin	Signal Name	I/O
1	Data carrier detect	I	2	Receive data#	I
3	Transmit data#	O	4	Data terminal read	O
5	Ground	NA	6	Data set ready	I
7	Request to send	O	8	Clear to send	I
9	Ring indicator	I			

Keyboard and Mouse Port Connectors

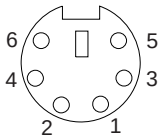


Figure 13. Keyboard and Mouse Port Connector

The keyboard and mouse ports each have a 6-pin, mini-DIN external connector.

Table 41. Pin Assignments for the Keyboard and Mouse Connectors

Pin	Signal Name	I/O	Pin	Signal Name	I/O
1	Data	I/O	2	Reserved	NA
3	Ground	NA	4	+5 V dc	NA
5	Clock	I/O	6	Reserved	NA

Monitor Port Connector

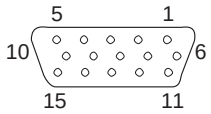


Figure 14. Monitor Connector

The external interface for the video subsystem is a 15-pin, female, D-shell, DDC2B-compliant connector located at the rear of the graphics adapter.

Table 42. Pin Assignments for the Monitor Connector

Pin	Signal Name	I/O
1	Red	O
2	Green	O
3	Blue	O
4	Monitor ID2 - not used	I
5	Ground	NA
6	Red ground	NA
7	Green ground	NA
8	Blue ground	NA
9	+5 V, used by DDC2B	NA
10	Ground	NA
11	Monitor ID 0 - not used	I
12	DDC2B serial data	I/O
13	Horizontal sync.	O
14	Vertical sync.	O
15	DDC2B clock	I/O

Note: All inputs and outputs are with respect to the system board.

Ethernet Connector

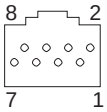


Figure 15. Ethernet Connector

The external interface for the Ethernet port is an 8-pin, RJ-45 connector.

Table 43. Pin Assignments for the Ethernet Connector

Pin	Signal Name	I/O
1	TxD+	O
2	TxD–	O
3	RxD+	I
4	Ground	NA
5	Ground	NA
6	RxD–	I
7	Ground	NA
8	Ground	NA

Appendix B. System Address Maps

System Memory Map

Memory can be mapped differently if POST detects an error.

Table 44. System Memory Map (Fixed Address Ranges)

Address Range (Dec)	Address Range (Hex)	Size	Description
0–511 KB	00000–7FFFF	512 KB	Conventional
512 KB–638 KB	80000–9FBFF	127 KB	Extended conventional
639 KB	9FC00–9FFFF	1 KB	Extended BIOS data (moveable by HIMEM, QEMM, 386MAX)
640 KB–767 KB	A0000–BFFF	128 KB	Video RAM
768 KB–799 KB	C0000–C7FFF	32 KB	Video ROM BIOS (shadowed)
800 KB–895 KB	C8000–DFFFF	96 KB	PCI/ISA space – available to ISA adapter ROMs
896 KB–1 MB	E0000–EFFFF F0000–FFFFF	128 KB	System POST only - available after boot ROM BIOS
1 MB–16 MB	100000–FFFFFF	15 MB	PCI/ISA space
16 MB–4095.872 MB	1000000–FFFDFFFF	4079.9 MB	PCI space (positive decode)
4095.872 MB–4096 (4 GB)	FFFE0000–FFFFFFFF	128 KB	System ROM BIOS (ISA bus)

Input/Output Address Map

The following table lists resource assignments for the I/O address map. Any addresses that are not shown are reserved.

Table 45 (Page 1 of 2). Input/Output Address Map

Address (Hex)	Size (Dec)	Description
0000–001F	32 bytes	DMA 1
0020–002D 0030–003F	30 bytes	Interrupt controller 1
002E–002F	2 bytes	Super I/O controller system board Plug-and-Play index/data registers (index=002E, data=002F)
0040–0043 0050–0053	8 bytes	Counter/timer 1
0044–004F 0054–005F	24 bytes	General I/O locations—available to ISA bus
0060	1 byte	Keyboard controller, data byte (on ISA data bus)
0061	1 byte	System port B
0064	1 byte	Keyboard controller, command and status byte (on ISA data bus)
0062, 0063, 0065–006F	13 bytes	General I/O locations—available to ISA bus
0070, bit 7 write only	1 bit	Enable/disable NMI
0070, bits 6—0	7 bits	Real-time clock, address (on ISA bus)
0071	1 byte	Real-time clock, data (on ISA bus)
0072—0077	6 bytes	Real-time clock, addresses and data
0078	4 bytes	General purpose I/O (GPIO)
007C	4 bytes	General purpose I/O (GPIO)
0080	1 byte	POST checkpoint register during POST only
0080–008F	16 bytes	DMA page registers
0090–009F	16 bytes	General I/O locations—available to ISA bus
00A0–00B1 00B4–00BF	30 bytes	Interrupt controller 2
00B2	1 byte	Advanced power management control
00B3	1 byte	Advanced power management status
00C0–00DF	32 bytes	DMA 2
00E0–00EF	16 bytes	General I/O locations—availabe to ISA bus
00F0	1 byte	Coprocessor error register
00F1–00FF	15 bytes	General I/O locations—available to ISA bus
0170–0177	8 bytes	IDE channel 1
01F0–01F7	8 bytes	IDE channel 0
0220–0227	8 bytes	Audio
0278–027F	8 bytes	LPT3
02E8–02EF	8 bytes	COM4
02F8–02FF	8 bytes	COM2
0376–0377	2 bytes	IDE channel 1
0378–037F	8 bytes	LPT2
03BC–03BE	4 bytes	LPT1 (system board)

Table 45 (Page 2 of 2). Input/Output Address Map

Address (Hex)	Size (Dec)	Description
03E8–03EF	8 bytes	COM3
03F0–03F5	6 bytes	Floppy channel 0
03F6	1 byte	IDE channel 0
03F7, bit 7	1 bit	Floppy disk change
03F7, bits 6:0	7 bits	IDE status channel 0
03F8–03FF	8 bytes	COM1
04D0	1 byte	Interrupt edge/level control 1
04D1	1 byte	Interrupt edge/level control 2
0CF8–0CFB	4 bytes	PCI configuration address register
0CF9	1 byte	Reset control register
0CFC–0CFF	4 bytes	PCI configuration data register

DMA I/O Address Map

The following table lists resource assignments for the DMA address map. Any addresses that are not shown are reserved.

Table 46 (Page 1 of 2). DMA I/O Addresses

Address (Hex)	Description	Bits	Byte Pointer
0000	Channel 0, Memory Address register	00–15	Yes
0001	Channel 0, Transfer Count register	00–15	Yes
0002	Channel 1, Memory Address register	00–15	Yes
0003	Channel 1, Transfer Count register	00–15	Yes
0004	Channel 2, Memory Address register	00–15	Yes
0005	Channel 2, Transfer Count register	00–15	Yes
0006	Channel 3, Memory Address register	00–15	Yes
0007	Channel 3, Transfer Count register	00–15	Yes
0008	Channels 0–3, Read Status/Write Command register	00–07	
0009	Channels 0–3, Write Request register	00–02	
000A	Channels 0–3, Write Single Mask register bits	00–02	
000B	Channels 0–3, Mode register (write)	00–07	
000C	Channels 0–3, Clear byte pointer (write)	NA	
000D	Channels 0–3, Master clear (write)/temp (read)	00–07	
000E	Channels 0–3, Clear Mask register (write)	00–03	
000F	Channels 0–3, Write All Mask register bits	00–03	
0081	Channel 2, Page Table Address register[8]	00–07	
0082	Channel 3, Page Table Address register[8]	00–07	
0083	Channel 1, Page Table Address register[8]	00–07	
0087	Channel 0, Page Table Address register[8]	00–07	
0089	Channel 6, Page Table Address register[8]	00–07	
008A	Channel 7, Page Table Address register[8]	00–07	
008B	Channel 5, Page Table Address register[8]	00–07	
008F	Channel 4, Page Table Address/Refresh register	00–07	
00C0	Channel 4, Memory Address register	00–15	Yes
00C2	Channel 4, Transfer Count register	00–15	Yes
00C4	Channel 5, Memory Address register	00–15	Yes
00C6	Channel 5, Transfer Count register	00–15	Yes
00C8	Channel 6, Memory Address register	00–15	Yes
00CA	Channel 6, Transfer Count register	00–15	Yes
00CC	Channel 7, Memory Address register	00–15	Yes
00CE	Channel 7, Transfer Count register	00–15	Yes
00D0	Channels 4–7, Read Status/Write Command register	00–07	
00D2	Channels 4–7, Write Request register	00–02	
00D4	Channels 4–7, Write Single Mask register bit	00–02	

[8] Upper byte of memory address register.

Table 46 (Page 2 of 2). DMA I/O Addresses

Address (Hex)	Description	Bits	Byte Pointer
00D6	Channels 4–7, Mode register (write)	00–07	
00D8	Channels 4–7, Clear byte pointer (write)	NA	
00DA	Channels 4–7, Master clear (write)/temp (read)	00–07	
00DC	Channels 4–7, Clear Mask register (write)	00–03	
00DE	Channels 4–7, Write All Mask register bits	00–03	
00DF	Channels 5–7, 8- or 16-bit mode select	00–07	

Appendix C. IRQ and DMA Channel Assignments

The following tables list the IRQ (interrupt request) and DMA (direct memory access) channel assignments for IntelliStation Z Pro computers.

Table 47. IRQ Channel Assignments

IRQ	System Resource
NMI	Critical system error
SMI	System management interrupt – power management
0	Reserved, internal timer
1	Reserved, keyboard buffer full
2	Reserved, cascade interrupt from slave PIC
3	COM2, COM4 if enabled; otherwise, user available for ISA or PCI bus
4	COM1, COM3 if enabled; otherwise, user available for ISA bus
5	LPT3 if enabled; otherwise, user available for ISA or PCI bus
6	Diskette drive controller
7	LPT1, LPT2 if enabled; otherwise, user available for ISA bus
8	Reserved, real-time clock
9	ACPI if enabled; otherwise, user available for ISA or PCI bus
10	User available for ISA or PCI bus
11	User available for ISA or PCI bus
12	System board mouse port if enabled; otherwise, user available for ISA or PCI bus
13	Reserved, math coprocessor
14	IDE primary channel if enabled; otherwise user available for ISA or PCI bus
15	IDE secondary channel if enabled; otherwise user available for ISA or PCI bus

Note: Audio IRQ and DMA resources are required and are assigned by the Plug and Play BIOS or operating system.

Table 48. DMA Channel Assignments

DMA Channel	Data Width	System Resource
0	8 bits only	User available for ISA bus
1	8 bits only	User available for ISA bus
2	8 bits only	Reserved, floppy
3	8 bits only	Parallel port if ECP; otherwise user available for ISA bus
4		Reserved–cascade channel
5	16 bits only	User available for ISA bus
6	16 bits only	User available for ISA bus
7	16 bits only	User available for ISA bus

Note: Channels 0–3 can transfer data in 64 KB pages; channels 5–7 can transfer data in 128 KB pages.

Appendix D. Error Codes

The following tables list the POST error codes and beep error codes for the IntelliStation Z Pro.

POST Error Codes

POST error messages appear when POST finds problems with the hardware during power-on or when a change in the hardware configuration is found. POST error messages are 3-, 4-, 5-, 8-, or 12-character alphanumeric messages. An *x* in an error message can represent any number.

Table 49 (Page 1 of 2). POST Error Codes

Code	Description
101	Interrupt failure
102	Timer failure
106	System board failure
111	I/O parity error 2 (I/O channel check latch set)
114	External ROM checksum error
121	Hardware error
151	Real time clock failure
161	Bad CMOS Battery
162	CMOS RAM checksum/configuration error
163	Clock not updating
164	CMOS RAM memory size does not match
167	Clock not updating
168	Alert on LAN is not working correctly.
175	System board error
176	System cover has been removed.
177	An inventory violation occurred, such as a hardware component was removed. This error message is part of the AssetCare and Asset ID features of the computer.
184	Asset control antenna not detected.
186	System board or hardware security error
187	Administrator password and boot sequences have been cleared.
190	The computer chassis-intrusion detector was cleared. This is an informational message. No action is required.
201	Memory data error
202	Memory address line error 00-15
203	Memory address line error 16-23
301	Keyboard error
303	Keyboard to system board interface error
601	Diskette drive or controller error
602	Diskette IPL boot record not valid
604	Unsupported diskette drive installed
662	Diskette drive configuration error
762	Math coprocessor configuration error
11xx	Serial port error (xx = serial port number)

Table 49 (Page 2 of 2). POST Error Codes

Code	Description
1762	Hard disk configuration error
1780	Hard disk 0 failed
1781	Hard disk 1 failed
1782	Hard disk 2 failed
1783	Hard disk 3 failed
1800	A PCI adapter has requested an unavailable hardware interrupt.
1801	A PCI adapter has requested an unavailable memory resource.
1802	A PCI adapter has requested an unavailable I/O address space, or the adapter is defective.
1803	A PCI adapter has requested an unavailable memory address space, or the adapter is defective.
1804	A PCI adapter has requested unavailable memory addresses.
1805	PCI adapter ROM error
1880	A Plug and Play adapter has requested a hardware interrupt that is not available.
1881	A Plug and Play adapter has requested memory resources that are not available.
1882	A Plug and Play adapter has requested an I/O address that is not available, or the Plug and Play adapter might be defective.
1883	A Plug and Play adapter has requested a memory address that is not available, or the Plug and Play adapter might be defective.
1884	A Plug and Play adapter has requested a memory address that is not available.
1885	A Plug and Play adapter read-only memory (ROM) error occurred.
1886	A Plug and Play adapter has requested a DMA address that is not available.
1962	Boot sequence error
8603	Pointing device or system board error
I9990301	Hard disk failure

Beep Codes

For the following beep codes, the numbers indicate the sequence and number of beeps. For example, a "2-3-2" error symptom (a burst of two beeps, three beeps, then two beeps) indicates a memory module problem. An *x* in an error message can represent any number.

Table 50. Beep Codes

Beep Code	Probable Cause
1-1-3	CMOS write/read failure
1-1-4	BIOS ROM checksum failure
1-2-1	Programmable interval timer test failure
1-2-2	DMA initialization failure
1-2-3	DMA page register write/read test failure
1-2-4	RAM refresh verification failure
1-3-1	1st 64 K RAM test failure
1-3-2	1st 64 K RAM parity test failure
2-1-1	Slave DMA register test in progress or failure
2-1-2	Master DMA register test in progress or failure
2-1-3	Master interrupt mask register test failure
2-1-4	Slave interrupt mask register test failure
2-2-2	Keyboard controller test failure
2-3-2	Screen memory test in progress or failure
2-3-3	Screen retrace tests in progress or failure
3-1-1	Timer tick interrupt test failure
3-1-2	Interval timer channel 2 test failure
3-1-4	Time-of-Day clock test failure
3-2-4	Comparing CMOS memory size against actual
3-3-1	Memory size mismatch occurred

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References

General Sources

Advanced Power Management (APM) BIOS Interface Specification 1.2
Source: Intel Corporation

AT Attachment Interface with Extensions
Source: American National Standard of Accredited Standards Committee

Extended Capabilities Port: Specification Kit
Source: Microsoft Corporation

Intel Microprocessor and Peripheral Component Literature
Source: Intel Corporation

PCI BIOS Specification 2.1
Source: PCI Special Interest Group

PCI Local Bus Specification 2.1
Source: PCI Special Interest Group

Plug and Play BIOS Specification, Errata and Clarifications
Source: Microsoft Corporation

World Wide Web Sources

82440GX PCI and Memory Controller
Source: Intel Corporation; available at http://developer.intel.com/design/agpsets/440GX

82371SB PCI ISA IDE Xcelerator (PIIX4)
Source: Intel Corporation; available at http://developer.intel.com/design/pcisets/datashts/290562.htm

Plug and Play BIOS Specification 1.0a
Source: Microsoft Corporation; available at http://www.microsoft.com/hwdev

Universal Serial Bus Specifications
Source: http://www.usb.org

Video Electronics Standards Association 1.2
Source: http://www.vesa.org

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