SIS301 Datasheet

Preliminary

Rev. 0.91

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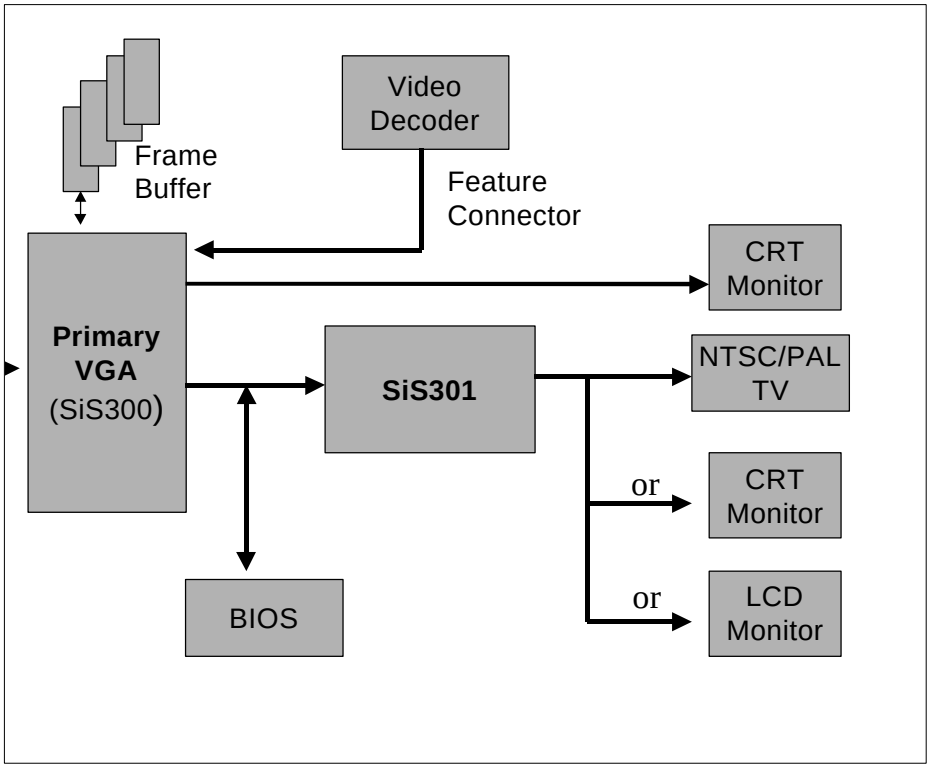
1 General Description

SiS301, which is an accompany chip of SiS VGA chip, integrates

- A NTSC/PAL video encoder with Macrovision Ver.7.1.L1 option for TV display.
- A TMDS™ transmitter with bi-linear scaling capability for TFT LCD panel display.
- An analog RGB port to support a secondary CRT monitor display.

All the above functions can support dual-display features. It means that the second display device driven by SiS301 can display independent resolutions, color depths and frame rates different from the primary VGA chip. SiS301 receives digital video signals and control signals from the primary VGA chip then transforms them into composite, S or component video output for TV display, TMDS™ signals for LCD display and analog RGB signals for secondary CRT display. The package type of SiS301 is 100-pin TQFP.

Figure 1-1 SiS301 Application Block Diagram



2 Features

2.1 TV Display

- Supports PAL and NTSC Systems.
- Supports Composite, S-Video, and Component R/G/B Output Signals
- Supports Component YUV Output for HiVision TV
- Supports Macrovision Copy Protection Process Rev. 7.1.L1
- Supports TV/Primary VGA Independent Display Resolution and Frame Rate at Enhanced Mode
- Provides Adaptive 6-Line Anti-Flicker Filtering.
- Provides Hardware Interpolation for Programmable Under-Scan/Over-Scan Adjustment.
- Provides Programmable Display Position Adjustment.
- Provides Programmable Notch Filter for Cross Color Elimination.
- Provides Chrominance Filter for Cross Luminance Elimination
- Provides Edge Enhancement Function for Better Text Quality.
- Provides Gamma Correction Independent of That of Primary VGA.
- Auto-Sense of TV Connection

2.2 TMDS™ Interfaced LCD Panel Display

- Supports TMDS™ Transmitter Function.
- Maximum Display Resolution 1280x1024@60NI.
- Supports TFT –24bit,TFT-18bit, TFT-12bit Monitor
- Provides Bi-Linear Scaling to Scale VGA Low Resolution Mode up for LCD Display.
- Supports LCD/Primary VGA Independent Display Resolution and Frame Rate at Enhanced Mode.
- Provides Programmable Display Centering.
- Compliant with VESA DDC2B
- Compliant with VESA Plug & Display, Hot Plugging Function.
- Compliant with VESA EDID3.0
- Provides Gamma Correction Independent of That of Primary VGA

2.3 Secondary CRT Display

- Supports Second CRT/Primary VGA Independent Display Resolution and Frame Rate at Enhanced Mode.
- Maximum Display Resolution: 1280x1024 @75NI, 135mhz
- Provides Gamma Correction Independent of That of Primary VGA.

3 Functional Description

Before going to the detailed functions of SiS301, let's introduce its two different operation modes which are master and slave mode, describing as following:

- **Master Mode**: SiS301 provides clock, horizontal sync, vertical sync signals to primary VGA. The CRT timing at primary VGA is gen-locked to these clock and control signals. This mode is selected when SiS301 performs TV or LCD display function. The CRT timing at primary VGA indicates the CRT1 (traditional CRT) at standard VGA modes and indicates the CRT2 (an extra CRT at SiS primary VGA) at enhanced modes.
- **Slave Modes**: SiS301 accepts horizontal sync, vertical sync signals from primary VGA. SiS301 provides clock to primary VGA CRT2 (or CRT1 at Standard Modes). The video data coming from primary VGA passes the RAMDAC for CRT display. This mode is selected when SiS301 performs Secondary CRT monitor display function.

3.1 TV Encoder

SiS301 integrates video encoder which supports NTSC/PAL and HiVision TV format. The output signal formats for NTSC/PAL system can be composite, S-video(Y/C), or RGB-component. The output signal format for HiVision TV is YUV-component output. The DAC resolution is 10-bits per channel. There are three sets of DAC implemented in SiS301.

The display on TV can be under-scan or over-scan mode. This function is supported by a flexible horizontal/vertical hardware scaling capability. The scaling factor is programmable. The maximum source resolution can be 800x600 for both NTSC and PAL and 1280X1024 for HiVision.

The Y/C filter implemented can reduce the cross-color and cross-luminance intervention. A SiS patented adaptive anti-flicker technology is implemented to remove the flicker but still retain the sharp profile. Another SiS developed technology which is called edge enhancement method(patent pending) is implemented to recover the sharpness after horizontal and vertical scaling.

Four analog comparators are integrated to detect the status of the TV connection. BIOS and software utility can set the video encoder configuration intelligently based on the read-back value. DAC power-down mode is automatically set according to the sense result.

The display at TV can be simultaneous and independent of the CRT output of primary VGA. When supporting TV display, SiS301 works at master mode. SiS301 sends the pixel clock, horizontal sync and vertical sync to primary VGA.

3.2 TMDS™ Interfaced LCD Display

SiS301 supports TMDS™ interfaced LCD panel display by implementing the transmitter inside. SiS301 receives parallel digital video data from a primary VGA. Through the use of DC balanced and transition minimized encoding and internal PLL, SiS301 encodes and serializes the input video data. The serialized data is then transmitted to the receiver chip over the Transition Minimized Differential Signaling (TMDS™) interconnection layer.

The output from SiS301 composes of three high speed data channels, TX2, TX1, and TX0 (for video data R, G, B respectively) and one low speed clock channel. The maximum output clock frequency is 110MHz, and the corresponding display resolution is 1280x1024@60Hz. There is built-in bi-linear scaling and centering function for low resolution image display.

When supporting LCD monitor display, SiS301 works at master mode. SiS301 outputs the pixel clock, horizontal sync and vertical sync to the primary VGA.

3.3 Secondary CRT Display

SiS301 integrates the VGA RAMDAC to support second CRT monitor display. SiS301 receives the parallel pixel data from primary VGA and passes them through RAMDAC to DAC output. The display at second VGA monitor can be simultaneous and independent of the CRT output of primary VGA.

When supporting second CRT monitor display, SiS301 works at slave mode. SiS301 receives the horizontal sync and vertical sync from primary VGA.

3.4 Display Modes

3.4.1 TV Output Modes

The table below lists part of the display modes supported by SiS301. The maximum input active resolution at PAL and NTSC system is 800x600. Because of the flexible scaling hardware, the over/under-scan (Active TV lines) modes supported by SiS301are far beyond of these listed data below.

System	Input(Active) Resolution	Active TV lines	Over/Under scan
NTSC	320x200	480 ~ 400	+
NTSC	640x480	480 ~ 400	+
NTSC	720x480	480 ~ 400	**+**
NTSC	720x400	480 ~ 400	**+**
NTSC	800x600	480 ~ 420	**+**

System	Input(Active) Resolution	Active TV lines	Over/Under scan
PAL	320x200	540 ~ 500	+
PAL	640x480	540 ~ 500	+
PAL	720x400	540 ~ 500	+
PAL	720x576	576 ~ 510	+
PAL	800x600	600 ~ 510	+

System	Input(Active) Resolution	Active TV Lines	Over/Under scan
HiVision	640x400	960	-
HiVision	640x480	960	-
HiVision	852x480	960	-
HiVision	1280x960	960 ~ 1032	+

3.4.2 LCD Output Modes

Display Device	Input(Active) Resolution	Scaling
LCD 800x600	Standard VGA Modes	Yes
	Enhanced VGA Mode	
	640x480	Yes
	800x600	No
LCD 1024x768	Standard VGA Modes	Yes
	Enhanced VGA Mode	
	640x480	Yes
	800x600	Yes
	1024x768	No
LCD 1280x1024	Standard VGA Modes	Yes
	Enhanced VGA Mode	
	640x480	Yes
	800x600	Yes
	1024x768	Yes
	1280x1024	No

3.4.3 Second CRT monitor Display:

Modes	Support
Standard Modes	Mode 0~Mode 13
Enhanced Graphic Modes	Up to 1280x1024, 75NI

3.4.4 Dual Display Application

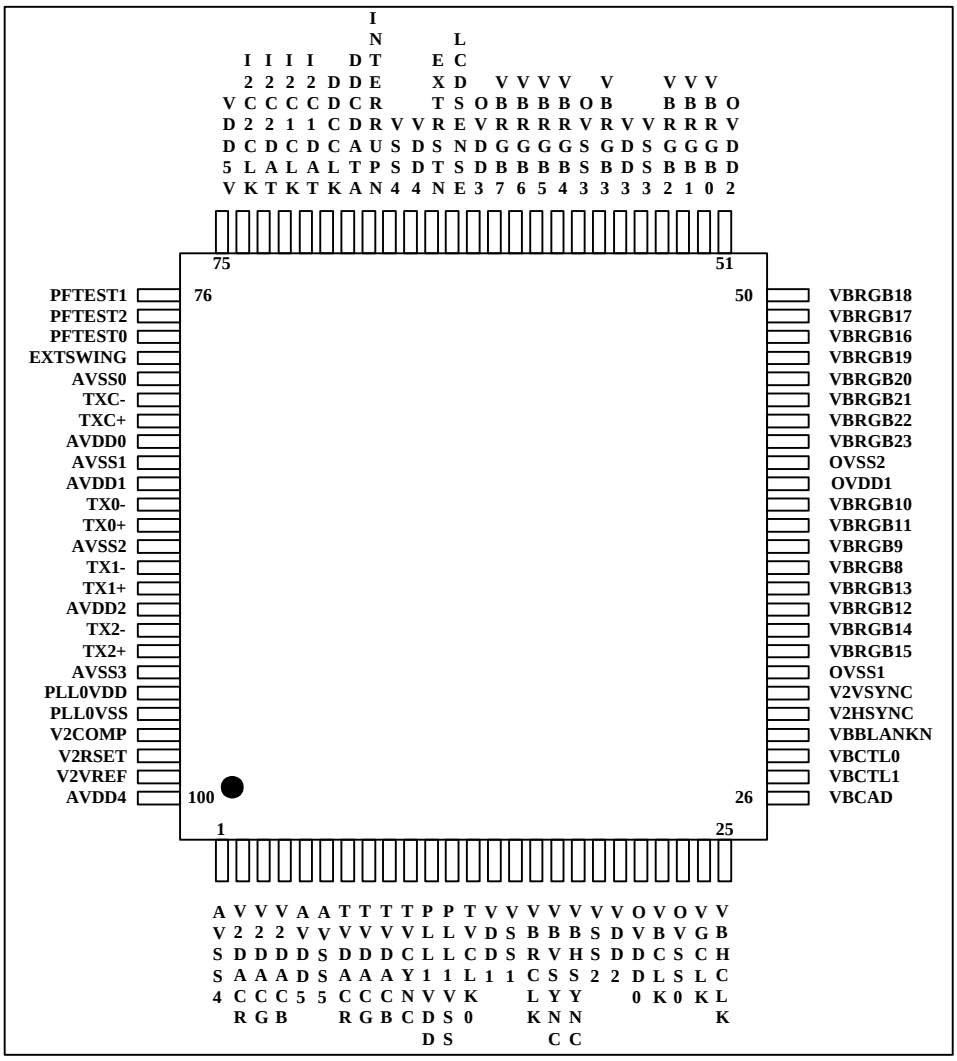
The table below illustrates the possible dual display applications.

Primary VGA Display	SiS301 Display	VGA Mode	Simultaneous View	Independent Dual Display (Frame Rate/ Display Buffer)	Under/ Overscan/ Scaling	H/V Position Adjustment
CRT	2nd CRT	Standard	Yes	No	No	Yes
CRT	2nd CRT	Enhanced Graphic	Yes	Yes	No	Yes

CRT	TV	Standard	Yes	No	No	Yes
CRT	TV	Enhanced Graphic	Yes	Yes	Yes	Yes
CRT	LCD	Standard	Yes	No	Yes	Yes
CRT	LCD	Enhanced Graphic	Yes	Yes	Yes	Yes
-	LCD only	Standard	-	-	Yes	Yes
-	LCD only	Enhanced Graphic	-	-	Yes	Yes
-	TV only	Standard	-	-	Yes	Yes
-	TV only	Enhanced Graphic	-	-	Yes	Yes

4 Pin Description

4.1 Pin Outline



4.2 Pin Description

Pin #	Pin Name	I/O Type	Description
25	VBHCLK	I	Register programming serial bus: clock

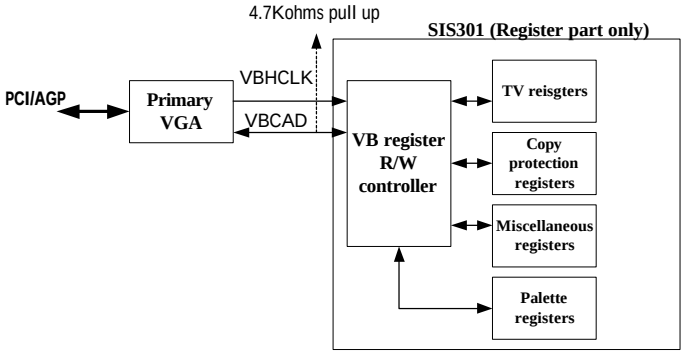
26	VBCAD	I/O	Register programming serial bus: command/address/data. External pull high.
43	VBRGB[23]	I	LCD/VGA/TV video data input: R[7]
44	VBRGB[22]	I	LCD/VGA/TV video data input: R[6]
45	VBRGB[21]	I	LCD/VGA/TV video data input: R[5]
46	VBRGB[20]	I	LCD/VGA/TV video data input: R[4]
47	VBRGB[19]	I	LCD/VGA/TV video data input: R[3]
50	VBRGB[18]	I	LCD/VGA/TV video data input: R[2]
49	VBRGB[17]	I	LCD/VGA/TV video data input: R[1]
48	VBRGB[16]	I	LCD/VGA/TV video data input: R[0]
33	VBRGB[15]	I	LCD/VGA/TV video data input: G[7]
34	VBRGB[14]	I	LCD/VGA/TV video data input: G[6]
36	VBRGB[13]	I	LCD/VGA/TV video data input: G[5]
35	VBRGB[12]	I	LCD/VGA/TV video data input: G[4]
39	VBRGB[11]	I	LCD/VGA/TV video data input: G[3]
40	VBRGB[10]	I	LCD/VGA/TV video data input: G[2]
38	VBRGB[9]	I	LCD/VGA/TV video data input: G[1]
37	VBRGB[8]	I	LCD/VGA/TV video data input: G[0]
62	VBRGB[7]	I	LCD/VGA/TV video data input: B[7]
61	VBRGB[6]	I	LCD/VGA/TV video data input: B[6]
60	VBRGB[5]	I	LCD/VGA/TV video data input: B[5]
59	VBRGB[4]	I	LCD/VGA/TV video data input: B[4]
57	VBRGB[3]	I	LCD/VGA/TV video data input: B[3]
54	VBRGB[2]	I	LCD/VGA/TV video data input: B[2]
53	VBRGB[1]	I	LCD/VGA/TV video data input: B[1]
52	VBRGB[0]	I	LCD/VGA/TV video data input: B[0]
24	VGCLK	I	Clock input from primary VGA
22	VBCLK	I/O	Clock output to primary VGA
18	VBHSYNC	I/O	Horizontal SYNC. Active high. Input from primary VGA at slave mode. Output to primary VGA at master mode.
17	VBVSYNC	I/O	Vertical SYNC. Active high. Input from primary VGA at slave mode. Output to primary VGA at master mode.
29	VBBLANKN	I/O	Data valid indication bit. VBBLANKN is high when input video data are valid. Input from primary VGA.
28	VBCTL0	I/O	Video control bit 0. Input from primary VGA.
27	VBCTL1	I/O	Video control bit 1. Input from primary VGA
16	VBRCLK	I	Reference clock: 14.31818 MHz
30	V2HSYNC	I/O	HSYNC output to 2nd CRT monitor
31	V2VSYNC	I/O	VSYNC output to 2nd VGA monitor
79	EXTSWING	.A I	TMDS™ external voltage reference
82	TXC+ (DTXCKP)	A O	TMDS™ transmitter out : Clock channel
81	TXC- (DTXCKN)	A O	TMDS™ transmitter out : Clock channel
87	TX0+ (DTX0P)	A O	TMDS™ transmitter out : B channel
86	TX0- (DTX0N)	A O	TMDS™ transmitter out : B channel

90	TX1+ (DTX1P)	A O	TMDS™ transmitter out : G channel
89	TX1- (DTX1N)	A O	TMDS™ transmitter out : G channel
93	TX2+ (DTX2P)	A O	TMDS™ transmitter out : R channel
92	TX2- (DTX2N)	A O	TMDS™ transmitter out : R channel
97	V2COMP	A I	DAC compensation
98	V2RSET	A I	DAC reference resistor
99	V2VREF	A I	DAC voltage reference
2	V2DACR	A O	DAC output: Analog R output at CRT or SCART TV mode
3	V2DACG	A O	DAC output: Analog G output at CRT or SCART TV mode
4	V2DACB	A O	DAC output: Analog B output at CRT or SCART TV mode
7	TVDACR	A O	DAC output : Composite output at standard PAL/NTSC TV mode. Analog U output at HiVision TV mode
8	TVDACG	A O	DAC output : Y output at standard PAL/NTSC TV mode. Analog Y output at HiVision TV mode
9	TVDACB	A O	DAC output : C output at standard PAL/NTSC TV mode. Analog V output at HiVision TV mode
10	TVCSYNC	A O	DAC output : TV CSYNC output at SCART TV mode
64	LCDSENSE	I/O	LCD panel plugging sense. Connect to LCD DFT connector. Internal I/O buffer pull low.
65	EXTRSTN	I	External Reset
68	INTERRUPN	I/O	Interrupt request. Active low.
69	DDCDATA	I/O	I2C data for primary VGA. Connect to 1st CRT T-type connector
70	DDCCLK	I/O	I2C clock for primary VGA. Connect to 1st CRT T-type connector
71	I2C1DAT	I/O	I2C data for LCD monitor. Connect to LCD DFT connector
72	I2C1CLK	I/O	I2C clock for LCD monitor Connect to LCD DFT connector
73	I2C2DAT	I/O	I2C data for 2nd CRT monitor. Connect to 2nd CRT T-type connector
74	I2C2CLK	I/O	I2C clock for 2nd CRT monitor Connect to 2nd CRT T-type connector
21	OVDD0		VDD
23	OVSS0		VSS
41	OVDD1		VDD
32	OVSS1		VSS
51	OVDD2		VDD
42	OVSS2		VSS
63	OVDD3		VDD
58	OVSS3		VSS
14	IVDD1		VDD

15	IVSS1		VSS
20	IVDD2		VDD
19	IVSS2		VSS
56	IVDD3		VDD
55	IVSS3		VSS
66	IVDD4		VDD
67	IVSS4		VSS
95	PLL0VDD		AVDD: for TMDS™ transmitter
96	PLL0VSS		AVSS : for TMDS™ transmitter
11	PLL1VDD		AVDD: for internal PLL
12	PLL1VSS		AVSS: for internal PLL
83	AVDD0		AVDD: for TMDS™ transmitter
80	AVSS0		AVSS: for TMDS™ transmitter
85	AVDD1		AVDD: for TMDS™ transmitter
84	AVSS1		AVSS: for TMDS™ transmitter
91	AVDD2		AVDD: for TMDS™ transmitter
88	AVSS2		AVSS: for TMDS™ transmitter
94	AVSS3		AVSS: for TMDS™ transmitter
100	AVDD4		AVDD: for TV/VGA DAC
1	AVSS4		AVSS: for TV/VGA DAC
5	AVDD5		AVDD: for TV/VGA DAC
6	IVSS0		AVSS: for TV/VGA DAC
75	VDD5V		Power supply for I2C data and clock
76	PFTEST1	I	For testing . Default pull low.
77	PFTEST2	I	For testing. Default pull low
78	PFTESTO	I/O	For testing output.
13	TVCLKO	I/O	For testing output.

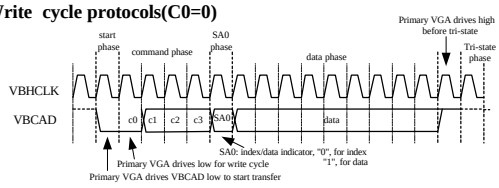
5 Register Programming Interface

SiS301 Register Programming Block Diagram



Transfer Protocol

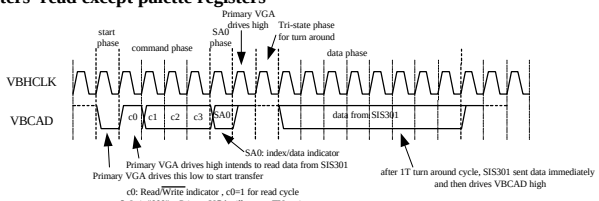
Write cycle protocols(C0=0)



c0: Read/Write indicator , c0=0 for write cycle
c3c2c1: "000" : Primary VGA will access TV registers
"001" : Primary VGA will access Copy protection registers
"010" : Primary VGA will access Miscellaneous registers
"011" : Primary VGA will access palette registers

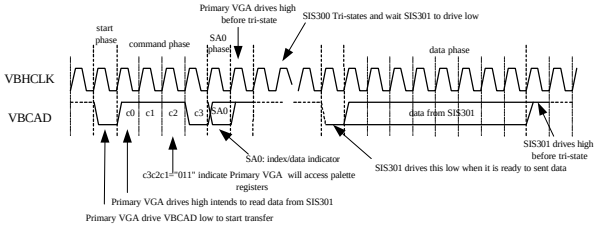
Read cycle protocols(C0=1)

a. registers read except palette registers



c0: Read/Write indicator , c0=1 for read cycle
c3c2c1: "000" : Primay VGAwill access TV registers
"001" : Primary VGA will access Copy protection registers
"010" : Primary VGA will access Miscellaneous registers

b. palette registers read



6 Electrical Characteristics

6.1 DC Characteristic

Table 6.1-1 Absolute Maximum Conditions

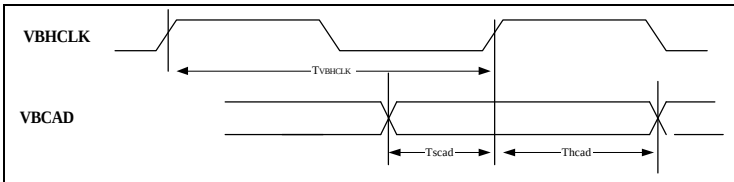
Symbol	Parameter	Min.	Max.	Units
Ta	Ambient Temperature	0	70	¢ J
Vcc	Supply Voltage 3.3V	-0.3	Vcc + 0.3	V
Vin	Input Voltage	-0.3	Vcc + 0.3	V
Vo	Output Voltage	-0.5	Vcc + 0.3	V
Pd	Package Power Dissipation	-	1.8	W

Table 6.1-1 DC Digital Specifications

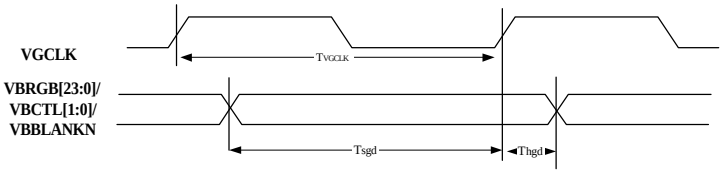
Symbol	Parameter	Min.	Max.	Units
Vil	Input Low Voltage	-0.5	0.8	V
Vih	Input High Voltage	2.2	Vcc + 10%	V
Vol	Output Low Voltage	-	0.4	V
Voh	Output High Voltage	2.4	-	V
Ili	Input Leakage Current	-	¡ Ó10	uA
Ito	Tristate Leakage Current	-	¡ Ó20	uA

6.2 AC Characteristic

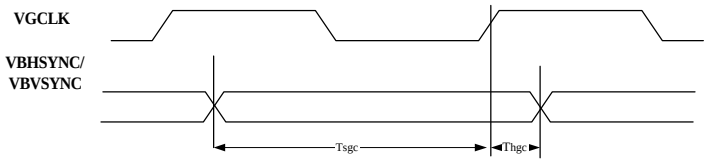
Symbol	Parameter	Min.	Max.	Units
T_{VBHCLK}	VBHCLK period	15	-	ns
T_{VGCLK}	VGCL:K period	7.4	-	ns
T_{VBCLK}	VBCLK period	7.4	-	ns
Tscad	VBCAD valid delay time	-	9	ns
Thcad	VBCAD valid preset time	-	3	ns
Tsgd	VBRGB[23:0], VBCTL[1:0], VBBLANKN setup time	2	-	ns
Thgd	VBRGB[23:0], VBCTL[1:0], VBBLANKN hold time	2	-	ns
Tsgc	VBHSYNC, VBVSYNC setup time at slave mode	2	-	ns
Thgc	VBHSYNC, VBVSYNC hold time at slave mode	2	-	ns
Tdctl	VBHSYNC, VBVSYNC output delay at master mode	-	TBD	ns



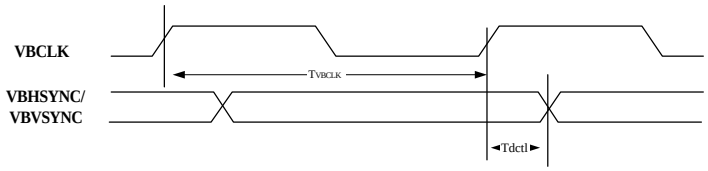
VBCAD timing relative to VBHCLK



VBRGB/VBCTL/VBBLANKN timing relative to VGCLK at SiS301 slave/master mode

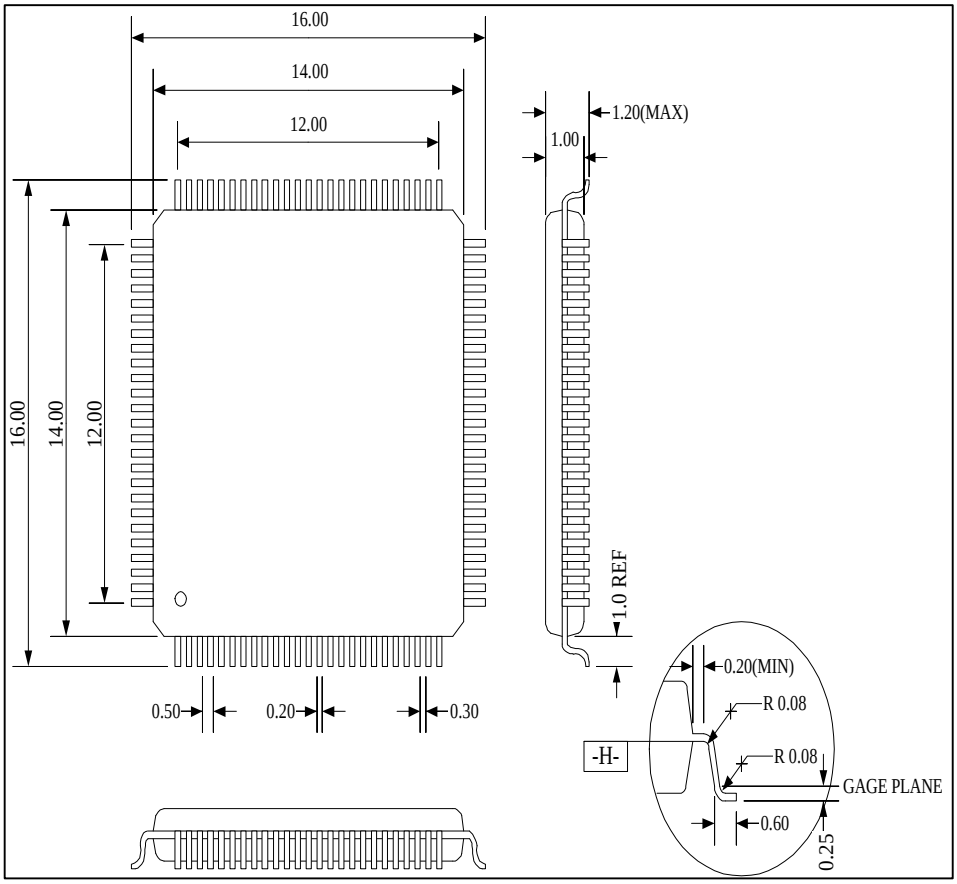


VBHSYNC/VBVSYNC timing relative to VGCLK at SiS301 slave mode



VBHSYNC/VBVSYNC timing relative to VBCLK at SiS301 master mode

7 Mechanical Dimension



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