IC WORKS

PRELIMINARY, MARCH 1995

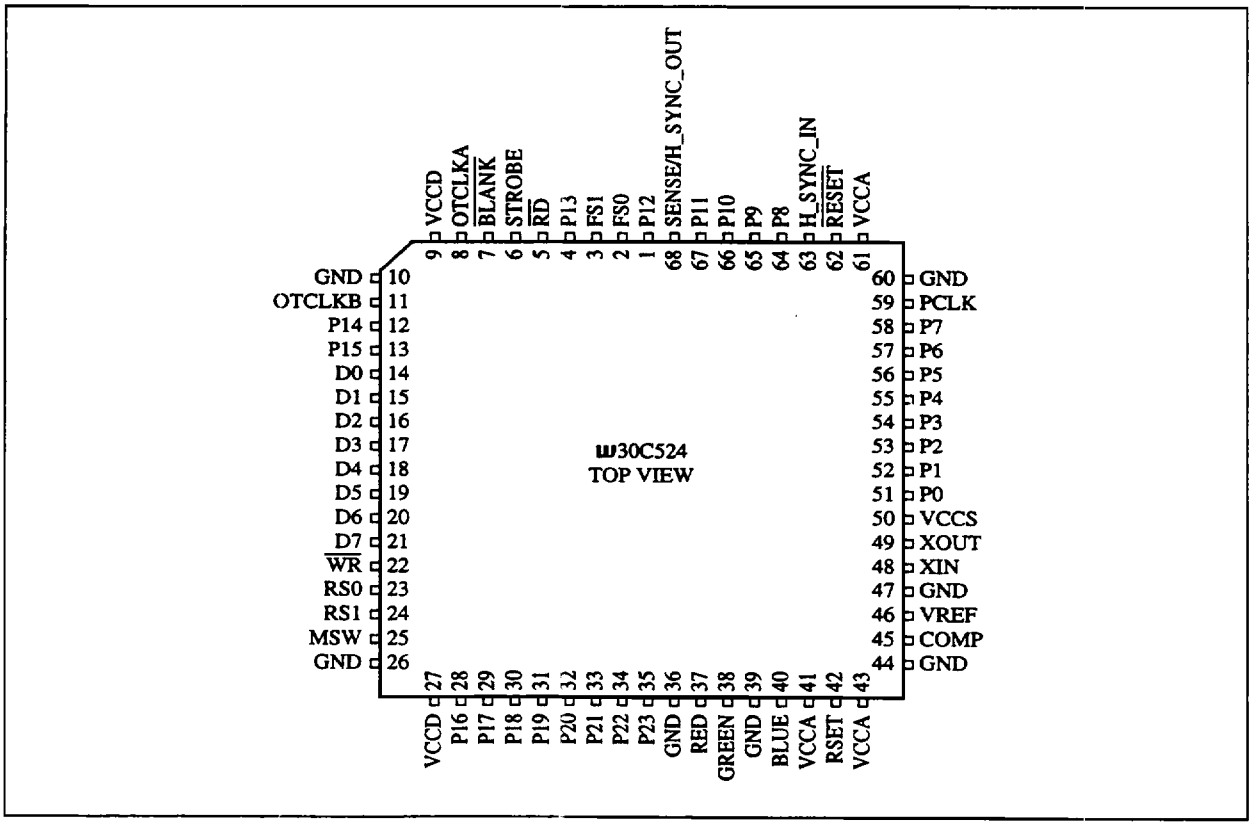
W30C524

DSP-based ZOOMDAC™ with Dual Clock Synthesizers

FEATURES

- Hardware 2-D Video Zoom
  - Resolutions up to 1280 x 1024
  - Non-Integer Ratios
  - From 1:1 to 32:1
  - Independent X and Y
  - 8, 15, 16 or 24 bit modes
- Hardware Video Filter
  - Resolutions up to 1280 x 1024
  - Zoom-tracking 2-D Digital Filter
  - Filters Non-Integer Zooms
  - 8, 15, 16 or 24 bit modes
  - For Software or Hardware Zoom
- 170, 135 and 110 MHz Versions
- Zoom/Filter up to 135 MHz
- 24-bit Pixel Port
- 8, 15, 16 or 24 bit-per-pixel modes
  - XGA™, HICOLOR™, TARGA™
  - Pixel-by-Pixel mode switching
- On-Chip clock doubler
- Dual programmable PLL clock synthesizers
- On-Chip Voltage Reference
- Software-readable output sense
- Device and manufacturer ID
- Delay Compensated Horiz. Sync
- Anti-Sparkle circuitry
- Low power 5 volt CMOS
- Power-Down for Battery and Green PCs
- 68-pin PLCC

FIGURE1: PIN DIAGRAM: W30C524



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TARGA is a trademark of Truevision Corp.
ZOOMDAC is a trademark of IC WORKS, Inc.
HICOLOR is a trademark of Sierra Semiconductor Corp.

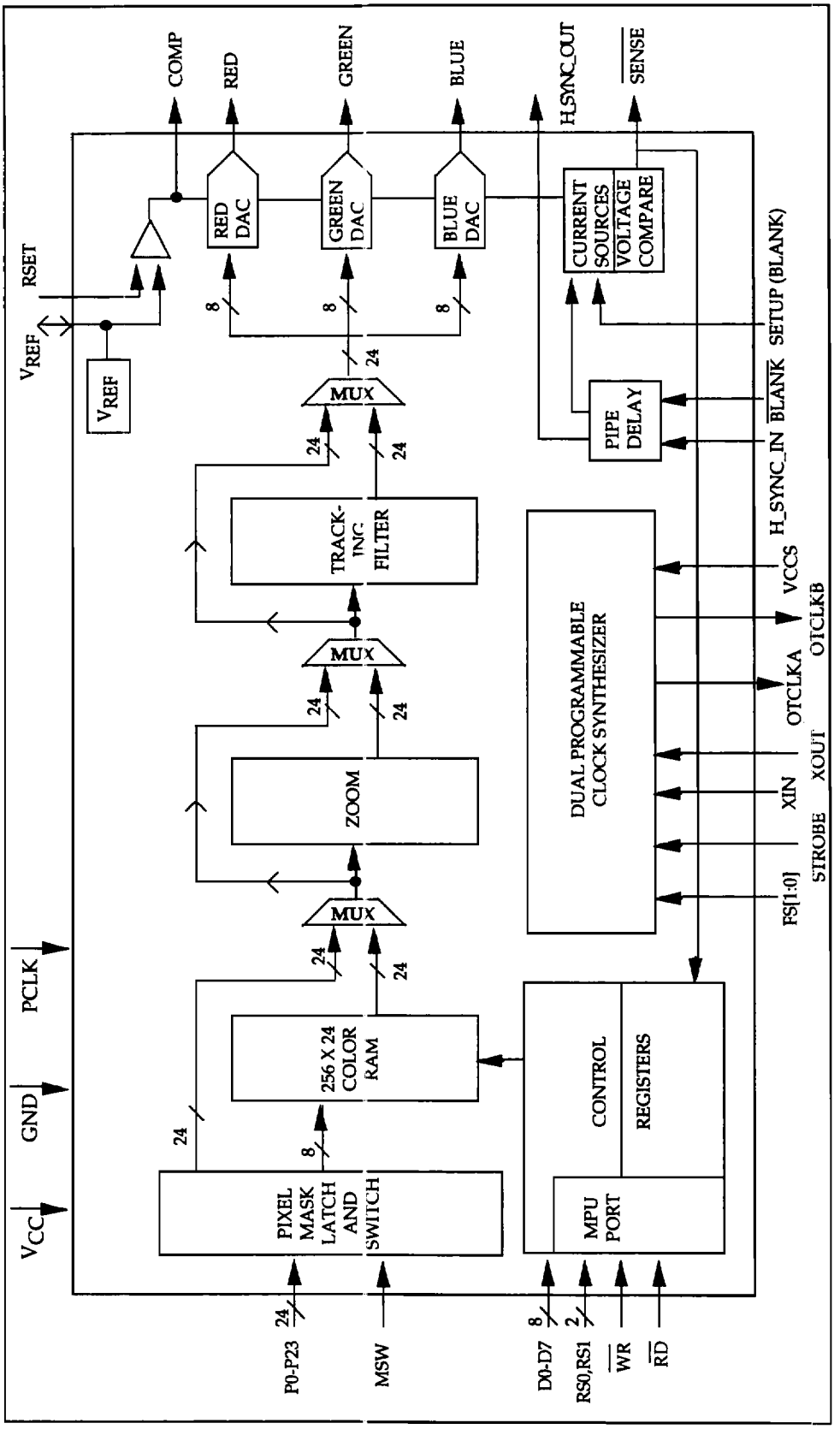

FIGURE 2: FUNCTIONAL BLOCK DIAGRAM: W30C524

APPLICATIONS

- **True-Color Super-VGA**
- **Add-in card or motherboard**
- **Desktop, Notebook and Green PC's**
- **Screen resolution up to:**
  - **1600 x 1200, 8-bit per pixel, 60Hz**
  - **1280 x 1024, 24-bit per pixel, 76Hz**
  - **1024 x 768, 24-bit pixel, 127Hz**
  - **800 x 600, 24-bit per pixel, 200Hz**

DESCRIPTION

The W30C524 is an advanced, high-performance super VGA RAM/DAC with dual programmable clock synthesizer specially enabled for Video for Windows, MPEG, and other video playback applications.

Built-in video zoom circuitry allows playback of larger video windows without sacrificing speed. An advanced 2-D tracking filter further enhances the video by removing the jagged zoom artifacts. The resulting video is enlarged and smooth without sacrificing frame rate.

A 24-bit pixel interface allows higher data throughput for more colors at higher screen resolutions. In 8-bit pixel modes, an on-chip 2-1 data multiplexer and on-chip clock doubler reduces external clock frequencies for easier FCC certification.

With 8, 15, 16 and 24 bit-per-pixel modes, the W30C524 supports all the major image formats, including XGA™, HICOLOR™ and TARGA™ formats. In addition to VGA compatible 18-bit modes to select 256 color look-up-table allows 8-bit modes to select 256 colors from the expanded 16 million color palette. Pixel-by-pixel mode switching allows mixing different image pixel formats on a single screen.

The device contains two programmable PLL clock synthesizers. Upon hardware reset, the clock synthesizers boot up to standard VGA and SVGA clock frequencies.

Software readable unique manufacturer and IC IDs allow for intelligent BIOS and plug-and-play board implementations.

Software controlled power-down modes are included for battery or green-PC applications.

Microsoft Windows is a registered trademark of Microsoft Corp.

XGA is a Trademark of International Business Machines Corp.
TARGA is a trademark of Truevision Corp.
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Table 1: Pin description

Pin Name	I/O	Pin #	Name/Function
VCCD	_	9, 27	Power, Digital. Connect these pins to +5 volts. These pins can be connected to the filtered supply plane or connected to the digital supply plane of the RAMDAC.
GND	--	10, 26, 36, 39, 44, 47, 60	Ground. Connect these pins to circuit ground.
VCCS	_	50	Power, Clock Synthesizer. Connect this pin to +5 volts. This can be a separate supply from the RAMDAC.
VCCA	--	41, 43, 61	Power, Analog. Connect this pin to +5 volts. These pins supply the power for the analog DACs and PLL portion of the clock synthesizers. This pin should be connected to a filtered supply plane.
P0-P23	I	51-58, 64-67, 1, 4, 12, 13, 28-35	Pixel Inputs: TTL compatible. These pins are latched on the rising edge of PCLK. Unused inputs should be connected to GND.
RSET	I	42	Reference: An external resistor (RSET) is connected between the RSET pin and GND to control the magnitude of the full-scale current.
COMP	I	45	Compensation Pin: Bypass this pin with an external 0.1µf capacitor to GND.
V_{REF}	--	46	Voltage Reference: Bypass this pin with an external 0.1µf capacitor to GND.
$\overline{\text{SENSE}}$ H_SYNC_OUT	O	68	$\overline{\text{SENSE}}$ or H_SYNC_OUT (Both Active-Low): TTL compatible. If Control Register [7] is "0" (powerup default), this pin functions as the monitor detect signal $\overline{\text{SENSE}}$ is a logic 0 if one or more of the red, green, or blue outputs has exceeded the internal voltage reference level of 340mV. If Control Register [7] is "1", this output pin changes function to become a delayed version of the H_SYNC_IN input signal. The delay is matched to the internal delays of the signal. The delay is matched to the internal delays of the W30C524 logic in all modes and this output is the preferred source with which to drive the CRT Horizontal Sync input.

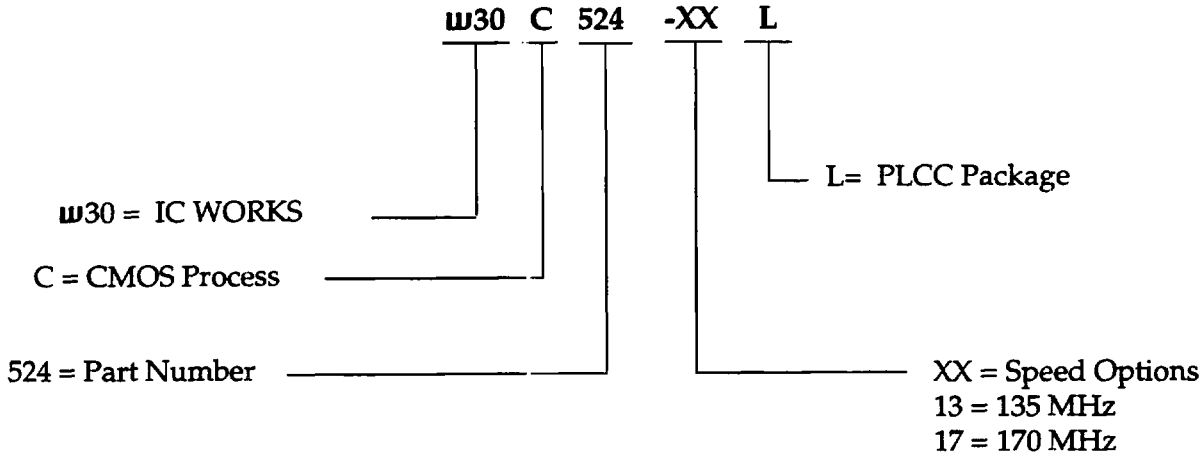
Table 1: Pin description (cont)

Pin Name	I/O	Pin #	Name/Function
PCLK	I	59	Pixel Clock: TTL compatible. The rising edge of the pixel clock latches the pixels, H_SYNC_IN and $\overline{\text{BLANK}}$ inputs.
$\overline{\text{BLANK}}$	I	7	Blank (Active-Low): TTL compatible $\overline{\text{BLANK}}$ is latched on the rising edge of PCLK. When $\overline{\text{BLANK}}$ is low, the 1.44mA current source on the analog outputs will be turned off and the DACs ignore digital input.
$\overline{\text{RESET}}$	I	62	TTL compatible. Resets internal registers to 0.
H_SYNC_IN	I	63	H_SYNC_IN is active low. In addition to providing synchronization for the internal zoom and filter logic, this input is delayed to latch the internal delays of the W30C524 and output as H_SYNC_IN to drive the monitor. H_SYNC_IN does not affect the video DAC levels.
D0-D7	I/O	14-21	Data Bus: TTL compatible. Data is transferred between the data bus and the internal registers under control of the $\overline{\text{RD}}$ and $\overline{\text{WR}}$ signals. In an MPU wire operation, D0-D7 is latched on the rising edge of $\overline{\text{WR}}$. To read data D0-D7 for the device $\overline{\text{RD}}$ must be in an active low state. The rising edge of the $\overline{\text{RD}}$ signal indicates the end of a read cycle. Following the read cycle, the data bus will to go a high impedance state. Note: for 6-bit operation, color data is contained in the lower six bits of the data bus. DO is the LSV and D5 is the MSB. When the MPU writes color data, D6 and D7 are ignored. During MPU read cycles, D6 and D7 are a logic 0.
$\overline{\text{WR}}$	I	22	Write (Active-Low): TTL compatible. $\overline{\text{WR}}$ controls the data transfer from the data bus to the selected internal register. D0-D7 data is latched at the rising edge of $\overline{\text{WR}}$, and RS0-RS1 data is latched at the falling edge of $\overline{\text{WR}}$.
$\overline{\text{RD}}$	I	5	Read (Active-Low): TTL Compatible. When $\overline{\text{RD}}$ is low, data transfers from the selected internal register to the data bus. RS0-RS1 is latched on the falling edge of $\overline{\text{RD}}$.
RS0-RS1	I	23, 24	Register Select: TTL compatible. These inputs are sampled on the falling edge of the $\overline{\text{RD}}$ or $\overline{\text{WR}}$ to determine which one of the internal registers is to be accessed.

Table 1: Pin description (cont)

Pin Name	I/O	Pin #	Name/Function
RED, GREEN, BLUE	I	37, 38, 40	Color Signals: These pins are analog outputs. High-impendance current sources are capable of driving a double-terminated 75 coaxial cable
MSW	I	25	Mode Switch: Input to change the RAMDAC mode. The RAMDAC interprets the incoming data on a pixel by pixel basis based on the mode. Ground if not used.
XIN	I	48	Crystal Input. Connect external crystal or stable frequency source to interrial crystal oscillator. The recommended frequency is 14.318 MHz system clock. When using a crystal, connect across XIN and XOUT.
XOUT	I	49	Crystal Ouput. Connect external crystal to internal crystal oscillator. All passive components are integrated on-chip to implement a tuned resonant circuit. Leave this pin floating when using a stable external frequency source connected to XIN.
OTCLKA	O	8	Ouput Clock A. TTL compatible. Output clock from analog PLL synthesizer A.
OTCLKB	O	11	Output Clock B. TTL compatible. Output clock from analog PLL synthesizer B.
FS[1:0]	I	3, 2	Frequency Select Lines. TTL compatible. Clock frequency select lines. These lines select the register set that determines the frequency of the clock synthesizers. The FS[1:0] pins select the register sets when CC[7] and CC[3] = 0. When CC[7] and CC[3] = 1, bits in the CC register select the register sets.
STROBE	I	6	STROBE. TTL compatible. Input for strobing the reference frequency select lines. FS[1:0] lines are connected to an internal transparent latch. When STROBE is high, data cannot be written to FS[1:0]. When STROBE is low, the latch is closed and data cannot be written to FS[1:0]. The falling edge of STROBE latches the FS[1:0] lines. If STROBE is tied permanently high, care must be taken to insure there is no noise or glitches on the FS[1:0] inputs.

ORDERING INFORMATION



VALID PART NUMBER

ω30C524 - 13L, ω30C524 - 17L

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