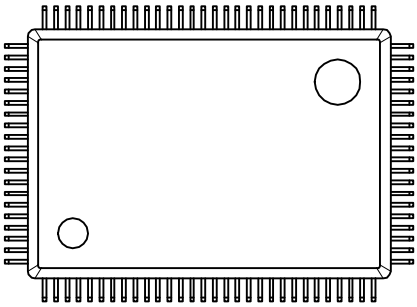
OVERVIEW

The **KS0164** wavetable synthesizer chip represents the state-of-the-art in multimedia audio technology. The **KS0164** combines a high-quality 32-voice wavetable synthesizer, a powerful 16-bit CPU and an MPU-401 compatibility into a single chip. The audio performance of a typical KS0164 system compares favorably to the best multimedia audio solutions available today, but at a fraction of the cost. A typical KS0164 system provides 32 voices of 16-bit, 44.1 kHz sample rate wavetable synthesis, MPU-401 compatibility, General MIDI, GS and MT-32 compatibility. With KS0164, a complete wavetable synthesizer may be implemented with as few as three ICs. Both serial and parallel MIDI interfaces are provided.

100 PQFP



FEATURES

- **High-quality 32-voice wavetable synthesizer**
- **General MIDI compliant**
- **Three serial output channels for addition of optional audio effects processor**
- **Supports all common CDP D/A formats**
- **Supports up to 24Mbytes of sample memory**
- **Supports 8-bit, 16-bit and compressed samples**
- **Directly supports ROM, SRAM and DRAM**
- **Hardware-based Roland MPU-401 emulation**
- **16-bit embedded CPU minimizes host PC overhead**
- **Integrated SRAM for embedded CPU**
- **Integrated MIDI UART**
- **Software-controlled SLEEP mode**
- **Sequoia Pegasus synthesizer firmware**
- **100 pin PQFP package**

ORDERING INFORMATION

Device	Package	Temperature Range
KS0164	100-QFP	0°~+70°C

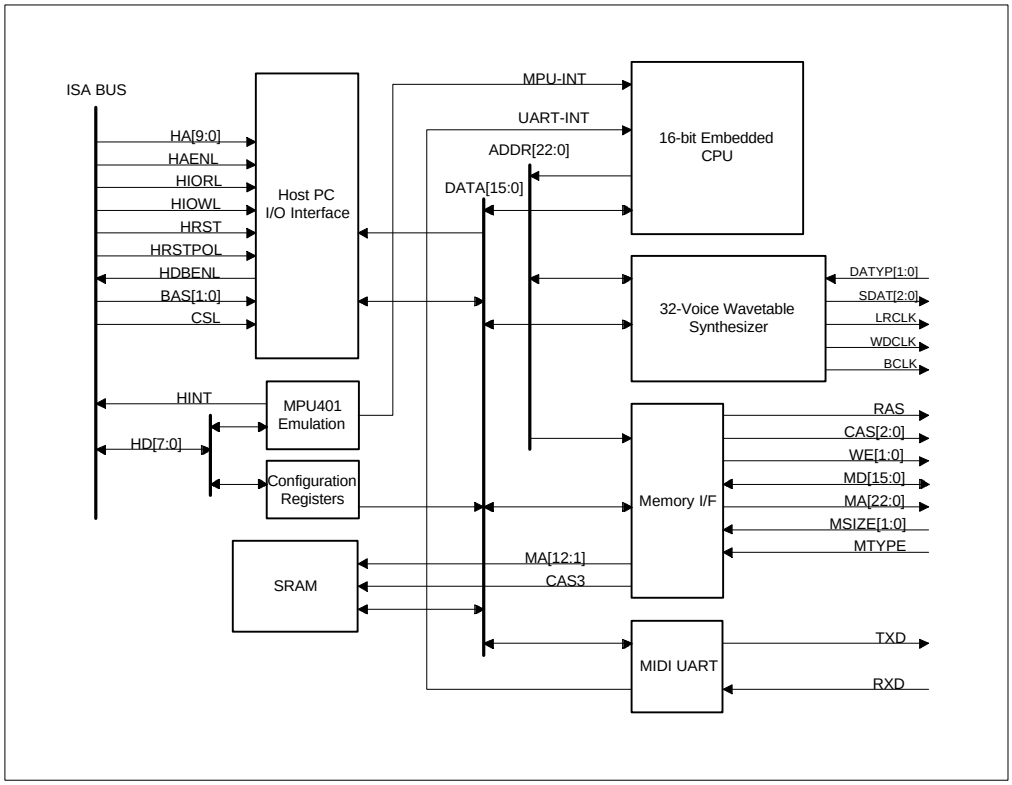
APPLICATIONS

- **MULTIMEDIA AUDIO PRODUCTS**
- **MUSICAL SYNTHESIZERS**
- **VIDEO GAME SOUND SYSTEMS**

RELATED PRODUCTS

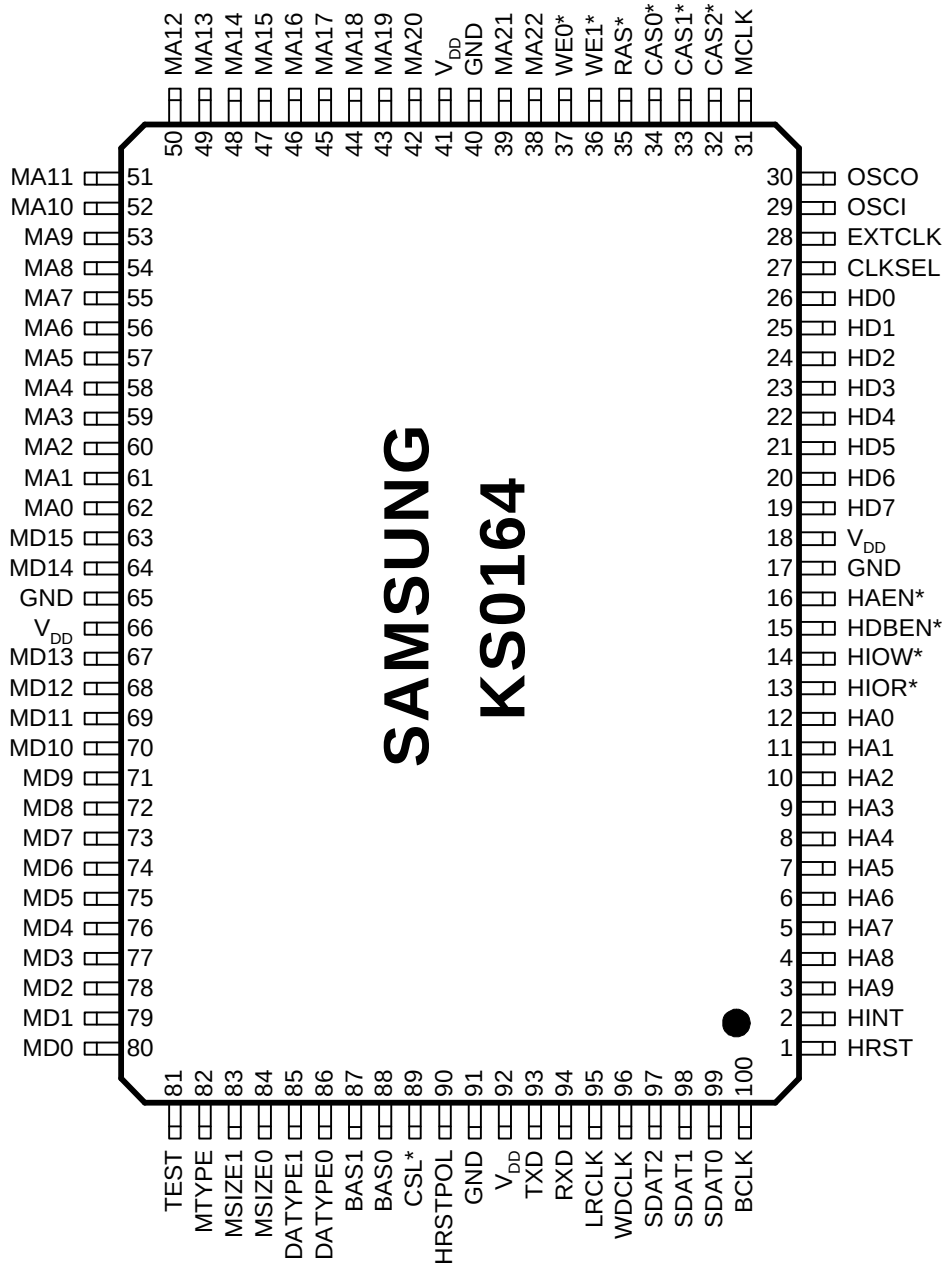
- **KS0174-1M 1MB Sample ROM**
- **KS0174-2M 2MB Sample ROM**
- **KS0174-4M 4MB Sample ROM**
- **KF353/D/S Dual Operational Amplifier**

BLOCK DIAGRAM



APPLICATION BLOCK DIAGRAM

PIN ASSIGNMENT - 100 PQFP



PIN ASSIGNMENT (Continued)

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
1	HRST	26	HD0	51	MA11	76	MD4
2	HINT	27	CLKSEL	52	MA10	77	MD3
3	HA9	28	EXTCLK	53	MA9	78	MD2
4	HA8	29	OSCI	54	MA8	79	MD1
5	HA7	30	OSCO	55	MA7	80	MD0
6	HA6	31	MCLK	56	MA6	81	TEST
7	HA5	32	CAS2*	57	MA5	82	MTYPE
8	HA4	33	CAS1*	58	MA4	83	MSIZE1
9	HA3	34	CAS0*	59	MA3	84	MSIZE0
10	HA2	35	RAS*	60	MA2	85	DATYPE1
11	HA1	36	WE1*	61	MA1	86	DATYPE0
12	HA0	37	WE0*	62	MA0	87	BAS1
13	HIOR*	38	MA22	63	MD15	88	BAS0
14	HIOW*	39	MA21	64	MD14	89	CSL*
15	HDBEN*	40	GND	65	GND	90	HRSTPOL
16	HAEN*	41	V_{DD}	66	V_{DD}	91	GND
17	GND	42	MA20	67	MD13	92	V_{DD}
18	V_{DD}	43	MA19	68	MD12	93	TXD
19	HD7	44	MA18	69	MD11	94	RXD
20	HD6	45	MA17	70	MD10	95	LRCLK
21	HD5	46	MA16	71	MD9	96	WDCLK
22	HD4	47	MA15	72	MD8	97	SDAT2
23	HD3	48	MA14	73	MD7	98	SDAT1
24	HD2	49	MA13	74	MD6	99	SDAT0
25	HD1	50	MA12	75	MD5	100	BCLK

PIN DESCRIPTION

Pin Name	*Pin #*	*Type*	*Description*
HOST PC INTERFACE			
HA9-0	3-12	I	Host Address Bits 9-0. These are the low 10 bits of the Host PC address bus, which are decoded to control access the MPU-401. For IBM PC application, these pins should be connected directly to A[9:0]. Alternatively, these pins may be tied to GND, and a fully qualified chip select signal may be connected to the CSL* pin instead.
HAEN*	16	I	Host Address Enable. This is the Host PC address decode enable. When Low, this signal enables the on-chip address decoder to decode HA[9:0], according to the base address selected by the BAS[1:0] signals. In this mode, the CSL* may be used instead. In this mode, only HA[3:0] will be decoded. For IBM-PC applications, this pin should be connected directly to AEN*.
BAS[1:0]	87,88	I	Base Address Select. These signals select the base address for the MPU-401 emulation as follows: 00b => 320-321H 01b => 330-331H 10b => 340-341H 11b => 350-351H
CSL*	89	I	Chip Select. For use at non-standard I/O addresses, or in applications where a chip select signal is available, HAEN* may be tied high, and the external chip select connected to CSL* instead. In this mode, only HA[3:0] are decoded on-chip.
HD[7:0]	19-26	I/O	Buffered Host PC Data Bus Bits [0:7].
HIOR*	13	I	Host I/O Read. This is the Host PC I/O read enable. The chip will only drive the HD[7:0] bus when a valid address decode is present, as determined by the HAEN*, BAS[1:0], and CSL* signals, and HIOR* is low.
HIOW*	14	I	Host I/O Write. This is the Host PC I/O write strobe. Data is written to internal registers on the rising edge of this signal.
HRST	1	I	Host PC Reset. The active polarity of this signal is determined by the HRSTPOL pin. For IBM PC application, this pin should be connected directly to the PC-bus RSTDRV signal. For daughter card applications, connect this pin to the reset signal from the host board.
HRSTPOL	90	I	HRST polarity select. This signal selects the active polarity for the HRST signal. When this pin is tied low, HRST will be active low.
HDBEN*	15	O	Host PC Data Bus Buffer Enable. This output controls the enable to the 74LS245 which buffers the Host PC data bus. This pin is driven low any time the MPU-401 is addressed for an I/O access.
HINT	2	O	Host MPU-401 Interrupt. This is a active high interrupt output from the MPU-401. It should be connected to one of the host IRQ lines, normally IRQ2.

Pin Name	*Pin #*	*Type*	*Description*
MEMORY INTERFACE			
MA[22:0]	38,39 42-62	O	Memory Address Bus Bits [22:0]. This is the external memory address bus. When accessing static memory devices (ROM/SRAM), these pins will contain a stable address throughout the entire memory cycle. When accessing dynamic memory, pins MA[11:0] will contain the multiplexed DRAM address.
MD[15:0]	63,64, 67-80	I/O	Memory Data Bus Bit [15:0]. This is the external memory data bus.
WE1*	36	O	Memory Upper Byte Write Enable. When this signal is low during an external memory access, it indicates that data bits MD[15:8] should be written to the addressed memory device.
WE0*	37	O	Memory Lower Byte Write Enable. When this signal is low during an external memory access, it indicates that data bits MD[7:0] should be written to the addressed memory device.
RAS*	35	O	Dynamic Memory Row Address Strobe. This signal is the Row Address Strobe for all external DRAM. When a DRAM device is addressed, this signal will be driven low shortly after the row address has been placed on MA[11:0]. It will also be driven low during ROM/SRAM cycles to provide CAS-before-RAS refresh for any DRAM devices in the system.
CAS*[2:0]	32-34	O	Dynamic Memory Column Address Strobes/Static Memory Chip Selects [2:0]. Up to three memory devices are supported. Device 0 must be a 16-bit wide ROM. Devices 1 and 2 may be either static or DRAM, although both must be the same type. The configuration of devices 1 and 2 is determined by the MSIZE and MTYPE[1:0] signals. When a DRAM device is addressed, one of these signals will be driven low shortly after the column address has been placed on MA0-11. It will also be driven low during static memory cycles to provide CAS-before-RAS refresh for any DRAM devices in the system. When a static device is addressed, one of these signals will be driven low shortly after the address has been placed on MA0-22.
MTYPE	82	I	Memory Type Select. This signal selects the type of memory device to be connected to CAS1* and/or CAS2*. When tied low, static memory devices are selected. When tied high, DRAM is selected.
MSIZE[1:0]	83,84	I	Dynamic Memory Size Select. If the MTYPE signal is tied high, these signals select the size of the DRAM devices connected to CAS1* and/or CAS2* as follows: 00b => 64K 01b => 256K 10b => 1M 11b => 4M
MCLK	31	O	Memory Clock. CPU and synthesizer external memory accesses are 1:1 interleaved. This signal indicates which device currently has control of the memory bus. When low, the CPU has control of the memory bus, when high, the synthesizer has control of the memory bus.

Pin Name	*Pin #*	*Type*	*Description*

D/A & EFFECTS PROCESSOR INTERFACE

SDAT[2:0]	97-99	O	D/A Converter Serial Data [2:0]. These are the three serial data outputs from the synthesizer core. Three outputs are provided so that one "dry" channel, and two separate effects channels can be provided by an external audio effects processor. In a minimum configuration, with no effects external processor, SDAT[0] would be connected to the data input of an external 16-bit stereo serial D/A converter, while SDAT[2:1] would be left unconnected.
BCLK	100	O	D/A Converter Bit Clock. This is the bit clock for the external serial D/A converter for the synthesizer.
LRCLK	95	O	D/A Converter L/R Clock. This is the L/R clock for the external serial D/A converter for the synthesizer.
WDCLK	96	O	D/A Converter Word Clock. This is the word clock for the external serial D/A Converter for the synthesizer.
DATYPE[1:0]	85,86	I	D/A Converter Serial Data Format Select. These signals select the data format of the D/A devices as follows: 00b => 32-bit Frame, I^2S (1 BCLK Delay) 01b => 32-bit Frame, (No Delay) 10b => 64-bit Frame, Left Justified 11b => 64-bit Frame, Right Justified (Japanese)

CLOCK INPUT

OSCI	29	I	16.9344 MHz Oscillator Buffer Input. This input will normally be connected to one side of a 16.9344MHz crystal, with a 20pF capacitor to ground. If desired, an externally generated 16.9344MHz clock may be connected to this pin instead. Note that due to internal analog circuitry, the chip may not behave reliably if this clock input is not close to the design frequency.
OSCO*	30	O	16.9344 MHz Oscillator Buffer Out. This input will normally be connected to one side of a 16.9344MHz crystal, with a 20pF capacitor to ground. If the OSCI pin is being driven by an externally generated clock, this pin should be left unconnected.
EXTCLK	28	I	External Clock Input. This input may be used to make use of an externally generated clock in place of the on-chip oscillator. This clock may be of any frequency up to 33MHz.
CLKSEL	27	I	External Clock Select. When this pin is low, the on-chip oscillator is disabled, and EXTCLK is used as the clock source for all on-chip timing. When high, the on-chip oscillator is enabled.

POWER AND GROUND

V_{DD}	18,41,66,92	+5V	Digital power supply.
GND	17,40,65,91	GND	Digital ground.

Pin Name	*Pin #*	*Type*	*Description*

MISCELLANEOUS

RXD	94	I	MIDI Receive Data. This is the TTL-level serial input to the 31.25 kBAUD MIDI UART. For normal MIDI communication, this pin must be driven by an external opto-isolator from the current-loop MIDI line.
TXD	93	O	TTL MIDI Transmit Data. This is the TTL-level serial output from the 31.25 kBAUD MIDI UART. For normal MIDI communication, this pin must drive an external voltage-to-current converter to drive the current-loop MIDI line.
TEST	81	I	Manufacturing Test Pin. For normal operation, this pin must be tied to GND. Applying power to the device with this pin floating or tied to a logic high level may cause permanent damage to the device

GENERAL DESCRIPTION

The **KS0164** is a highly integrated wavetable synthesizer chip, designed to be a part of a high-performance, low-cost multimedia audio systems. The chip contains a complete 32-voice, 16-bit, 44.1kHz wavetable synthesizer, a high-performance 16-bit CPU, extensive compatibility with established standard audio interfaces, all necessary system glue logic and total software configurability. With its on-chip CPU, a KS0164-based synthesizer imposes absolutely minimal host CPU overhead. Its hardware-based MPU-401 emulation completely eliminates the memory overhead, software compatibility and stability problems of TSR-based emulations. The following sections give a brief description of the major functional blocks of the KS0164.

HOST PC INTERFACE

All necessary ISA bus interface logic is completely contained on-chip. This includes address decoding for the MPU-401 emulation, control signal interpretation, and optional data bus buffer control. All PC interface control logic operates completely asynchronously to the synthesizer/CPU logic. Standard interfacing techniques are used to provide a highly compatible and reliable interface.

The MPU-401 emulation can be decoded for any one of four standard address ranges, as selected by the BAS[1:0] pins. In addition, a serial MIDI interface may be used, leaving the MPU-401 emulation inactive. This mode is particularly useful for stand-alone synthesizer modules and WaveBlaster-type daughter board applications.

To better support non-PC-based applications, including stand-alone applications where no host CPU is available, the reset signal polarity is programmable via the HRSTPOL pin, to accommodate existing active high or active low reset signals.

MPU-401 INTERFACE

One of the two available interfaces for communicating MIDI data to/from the KS0164 is the on-chip MPU-401 emulation. This emulation provides the full hardware functionality of a real MPU-401. MPU-401 UART mode is fully supported, while a subset of the "intelligent" mode commands are also supported. The intelligent-mode support currently provided is adequate to support nearly all existing MPU-401 applications.

MIDI UART INTERFACE

The second of the two available interfaces for communicating MIDI data to/from the KS0164 is the on-chip of MIDI UART. This interface is always active, and works independently from the MPU-401 emulation, allowing the KS0164 to easily be used in stand-alone MIDI modules and WaveBlaster-type daughter board applications.

EMBEDDED CPU

In sharp contrast to most other low-cost multimedia audio solutions currently available, the KS0164 does not rely on the host PC processor or an external microcontroller to drive the wavetable synthesizer. Rather, the KS0164 contains a high-performance purpose-built 16-bit CPU incorporating such advanced features as six different addressing modes, a hardware multiplier, a barrel shifter, and a peak execution rate of nearly 3 million instructions per second. In addition to providing optimal synthesizer audio quality, this reduces host PC CPU overhead. The considerable memory overhead, compatibility problems, and erratic audio quality associated with TSR-based solutions are also completely eliminated.

SYNTHESIZER

The synthesizer is a high-performance 32-voice, 16-bit wavetable synthesizer. While nearly all wavetable systems being offered today operate at sample rates ranging anywhere from 22-32kHz, the KS0164 performs all sample processing at a full 44.1 kHz. In addition, some other systems support only 12-bit samples. The KS0164, on the other hand, supports 8- and 16-bit linear samples, and 8- and 12-bit compressed samples. This allows nearly optimal tradeoffs between sample size and audio quality on a sample-by-sample basis in the design of the sample set, resulting in the best possible sound quality from a given total sample memory size.

GENERAL DESCRIPTION (continued)

The specification for the synthesizer are as follows:

Architecture:	Digital Wavetable Synthesizer
Voices:	32
Polyphony:	32 Notes Maximum
Multi-Timbral Capability:	Up To 16 Parts
Sample Memory:	Up To 16 MWords of ROM/SRAM/DRAM
Available Sample Sets:	2Mx16-bits, 1Mx16-bits, 512Kx16-bits
D/A Converter:	16-Bit Linear Serial Converter, All Common Data Formats Supported
Sample Playback Rate:	Fixed @ 44.1 kHz
Level And Panning Controls:	Separate 16-Bit L&R Volume Controls For Each Voice
Filters:	2 Separate 2-Pole Resonant Digital Filters For Each Voice
Data Formats:	8- Or 16-Bit Signed Linear Or 8- Or 12-Bit Compressed
Envelopes:	Hardware Envelopes For Amplitude and Filters
Effects:	Effects Loop Provided For DSP Multiple Effects Processor
Firmware:	Sequoia Development Group Pegasus Synthesizer Firmware
Compatibility:	Fully General-MIDI Compliant
	Roland MT-32 Sound Set Compatible

SYSTEM TIMING AND CONTROL

All timing is derived from a 16.9344 MHz crystal oscillator, or an externally generated oscillator of any frequency up to 33 MHz. However, note that the internal MIDI UART baud rate is directly proportional to the system clock rate. At any crystal frequency other than 16.9344 MHz, the UART baud rate will not be correct.

SAMPLE MEMORY INTERFACE

Each memory access cycle consists of 3 cycles of the 16.9344 MHz master clock, or 177.15 nsec. This is adequate to allow use of 150 nsec ROM, and 80 nsec DRAM. The memory interface supports a minimum of one and a maximum of three memory devices. In general the CPU will execute entirely out of ROM, and most, if not all, synthesizer voices will also be playing primarily from ROM, although entirely RAM-based systems are also fully supported. ROM memory accesses are exploited to allow DRAM refresh to occur simultaneously with ROM accesses by executing CAS-before-RAS refresh cycles on all DRAM banks in parallel with all ROM/SRAM accesses. For systems with ROM-based samples, this scheme provides adequate refresh for all DRAM in the system. For a totally DRAM-based system, it is necessary to allocate one synthesizer voice to perform DRAM refresh. For a combined ROM/DRAM system, as long as at least two voices are playing samples from ROM at all times, adequate refresh will be provided automatically, otherwise one voice must be dedicated to providing DRAM refresh.

REGISTER DESCRIPTION

DIRECT-ADDRESSED REGISTERS

MPU-401 DATA REGISTER **READ/WRITE**

ADDRESS	MNEMONIC	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BASE+0	HMAD	D7	D6	D5	D4	D3	D2	D1	D0

D[7:0]	MPU-401 A data.

MPU-401 COMMAND REGISTER **WRITE ONLY**

ADDRESS	MNEMONIC	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BASE+1	HMAC	C7	C6	C5	C4	C3	C2	C1	C0

C[7:0]	MPU-401 A command.

MPU-401 STATUS REGISTER **READ ONLY**

ADDRESS	MNEMONIC	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BASE+1	HMAC	RXRDY	TXRDY	1	1	1	1	1	1

RXRDY	Received Data Ready Status 0 = Received data is available in HMAD 1 = Received data is not available
TXRDY	Transmit Data Buffer Ready Status 0 = MPU-401 is ready to receive next data/command in HMAD or HMAC 1 = MPU-401 is not ready to receive next data/command

ELECTRICAL SPECIFICATION

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS	SYMBOL	MIN	MAX	UNIT
Supply Voltage (Measured To V_{SS})	V_{DD}	-0.5	+7.0	V
Input Voltage (Any Pin)	V_{IN}	V_{SS} -0.5	V_{DD}+0.5	V
Ambient Operating Temperature Range	T_{opr}	0	+70	°C
Storage Temperature Range	T_{stg}	-55	+150	°C

Notes:

1. Absolute maximum ratings are limiting values applied individually, while all other parameters are within specified operating conditions.
2. Functional operation under any of these conditions is not implied.

DC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage (Measured To GND)	V_{DD}	4.75	5.0	5.25	V
Input High Voltage	V_{IH}	2.2	-	V_{DD}+0.3	V
Input Low Voltage	V_{IL}	V_{SS}-0.3	-	0.8	V
Digital Output High Voltage (I_{OH}=400μA)	V_{OH}	2.4	-	-	V
Digital Output Low Voltage (I_{OL}=3.2mA)	V_{OL}	-	-	0.45	V
Input Leakage High Current	I_{IH}	-10	0	10	μA
Input Leakage Low Current*	I_{IL}	-10	0	10	μA
Supply Current	I_{CC}	-	100	250	mA
Pull-up Resistance**	R_{UP}	40	-	250	kΩ

Test Condition : V_{DD}=5.0V, V_{SS}=0V, f_{osc}=16.9344MHz, T_a=25°C

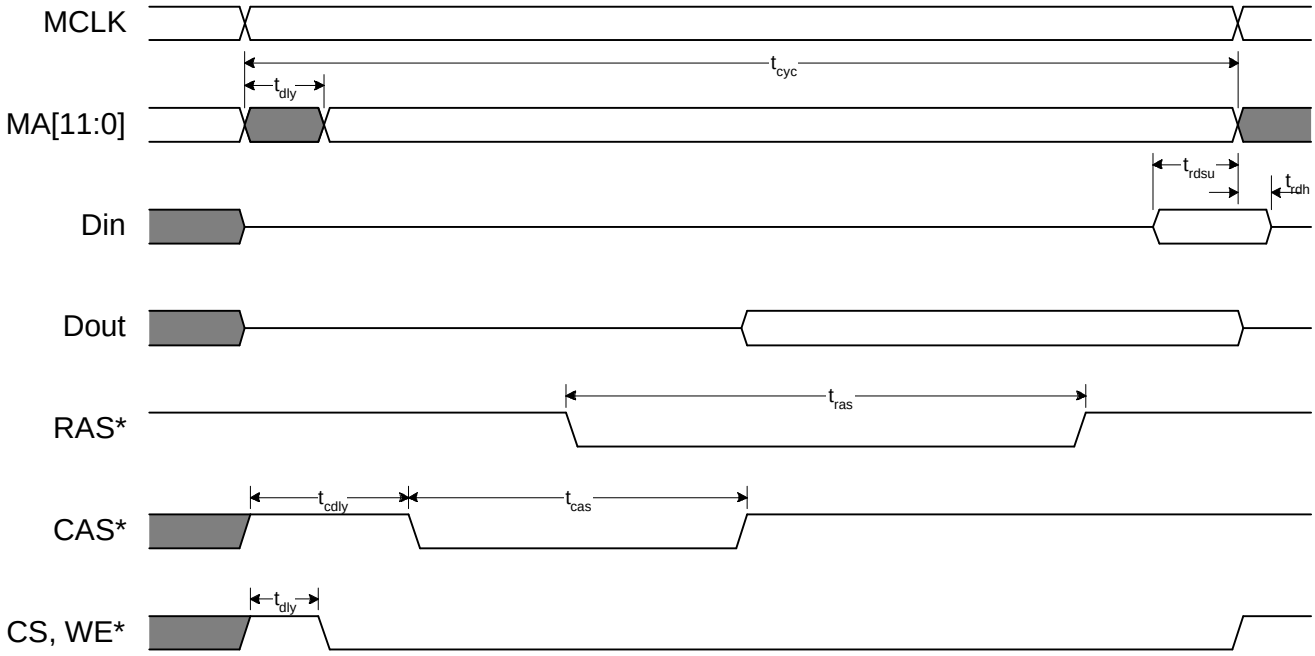
* For pins TEST, MTYPE, MSIZ[1:0], BAS[1:0], HRSTPOL, HRST, DATYPE[1:0] and CSL
** All input pins except ones in *

ELECTRICAL SPECIFICATION (continued)

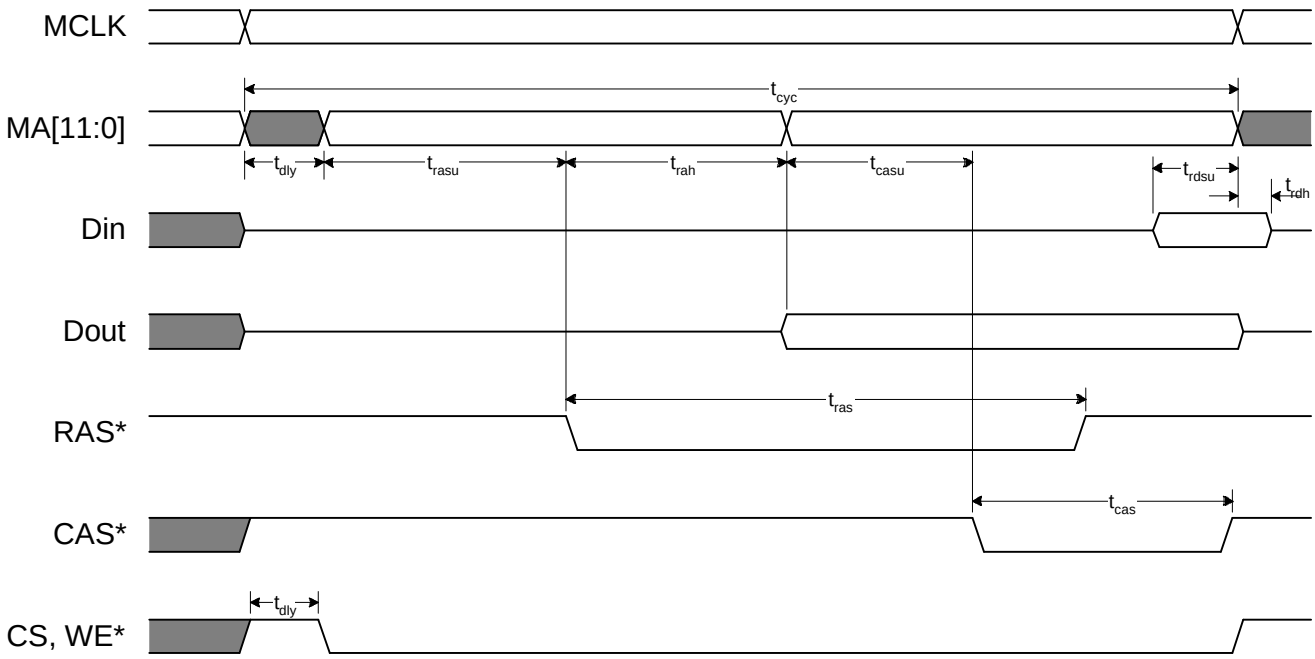
AC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	SYMBOL	MIN	TYP	MAX	UNIT
Memory Cycle Time	t_{cyc}	-	177	-	nsec
Memory Address/Control Delay	t_{dly}	-	15	-	nsec
Memory Read Data Setup Time	t_{rdsu}	15	-	-	nsec
Memory Read Data Hold Time	t_{rdh}	0	-	-	nsec
RAS* Active Time	t_{ras}	-	88	-	nsec
CAS* Active Delay Time	t_{cdly}	-	29	-	nsec
CAS* Active Time	t_{cas}	-	59	-	nsec
Row Address Setup Time	t_{rasu}	-	44	-	nsec
Row Address Hold Time	t_{rah}	-	29	-	nsec
Column Address Setup Time	t_{casu}	-	29	-	nsec
Oscillator Frequency	f_{osc}	-	-	16.9344	MHz

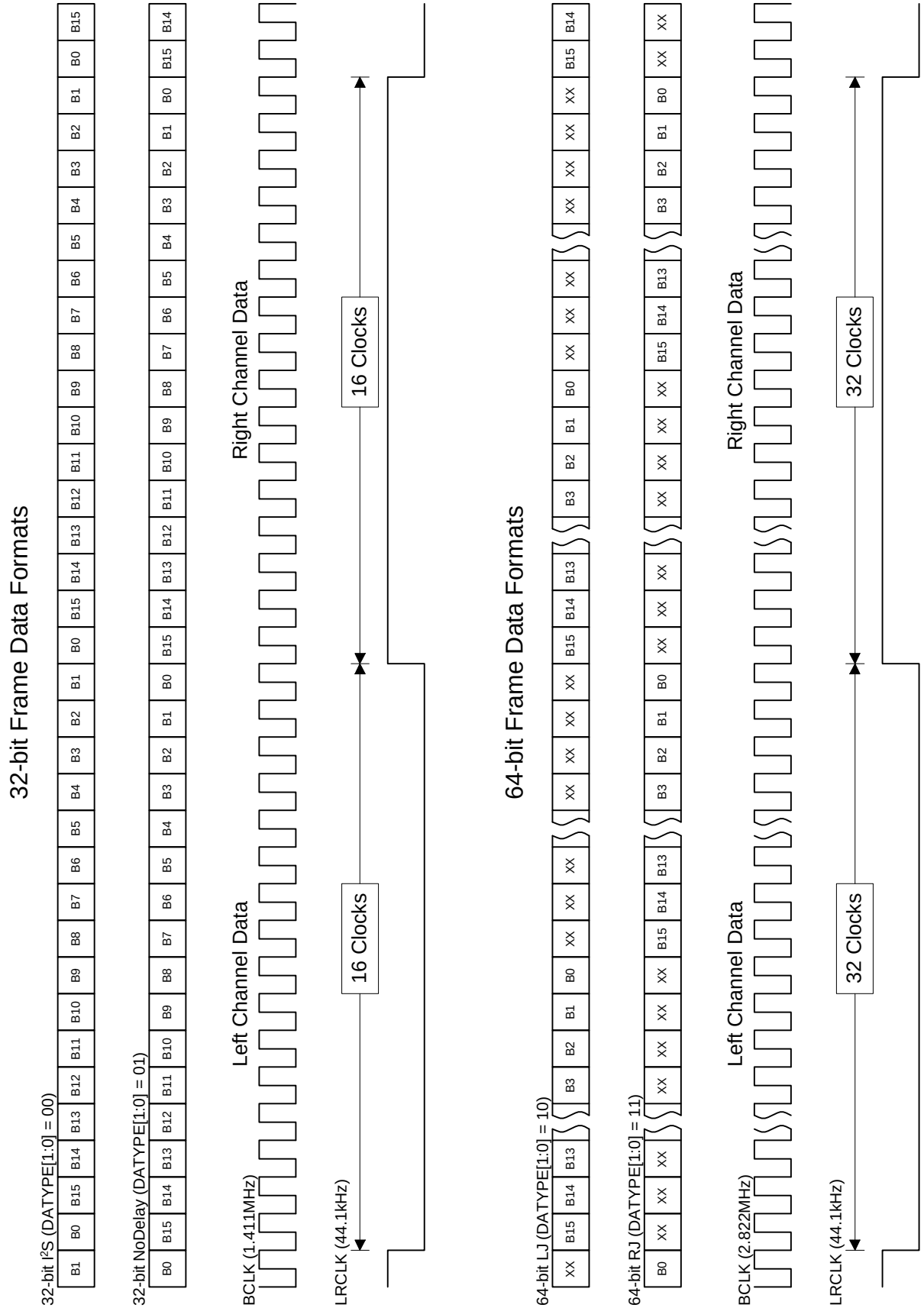
Test Condition : V_{DD}=5.0V, V_{SS}=0V, f_{osc}=16.9344MHz, T_a=25^oC



ROM/SRAM MEMORY INTERFACE TIMING



DRAM MEMORY INTERFACE TIMING



Audio Board Design & PCB Layout Guidelines

Overview

Proper analog circuit design and PCB layout are essential to achieving optimum audio performance, as well as acceptable EMI (FCC/VDE) characteristics from PC audio boards. This document outlines the basic guidelines that should be followed to ensure acceptable performance in these critical areas. As a reference, please refer to the evaluation board schematics and PCB layout.

Design Overview

In order to achieve optimum audio performance, in terms of signal-to-noise ratio, noise, floor, and distortion, always provide separate analog and digital supplies and grounds. All digital components should be connected to VCC and GND, directly from the PC bus connectors. Single-ended analog circuitry, such as D/A converters, CODECs, etc., should be operated from a separate +5V supply which is locally regulated down from the +12V supply available on the PC bus. All operational amplifiers should be powered by filtered ±12V supplies derived from the ±12V supplies available on the PC bus. Operational amplifiers should ***never*** be operated from a single-ended supply. This will not only reduce the dynamic range and headroom, but also significantly degrade the signal-to-noise ratio.

Handling Grounds

For optimum audio performance, it would be most desirable to keep the analog and digital supplies and returns totally isolated from one another. However, for the sake of EMI (FCC) performance, it is generally necessary to keep all supplies closely coupled. Also, in a PC, there are a limited number of supplies to work from, and only a single GND. These conflicting requirements are best met by allowing the digital and analog returns (GND & AGND) to be directly connected at only a single location, preferably directly adjacent to the card bracket. This single connection should be a substantial one, at least 100-200 mils. This connection is indicated in the Evaluation Board Schematics as a GNDSTRAP component. AC coupling the returns by means of 1-10nF capacitors straddling the perimeter of the AGND/GND planes, at intervals of no more than 1-1.5″, should provide the coupling necessary to prevent EMI problems which can be caused by the separate ground planes. The DB-15 connector shell must be securely connected to the GND plane, and the connector must be securely screwed to the bottom of the bracket, while the top of the bracket should have a tab which is securely screwed of riveted to the AGND plane, thus referencing all outgoing signal lines to the (relatively) clean chassis ground at the bracket. In past designs, these techniques have consistently resulted in a > 10dB margin relative to the FCC Class-B limits.

In the analog section, it is desirable to have two AGND planes, rather than a single AGND plane, and a single power plane. All analog supplies can be easily routed as normal traces, since the currents are very low. If possible, place the AGND planes on the outer layer, and do all signal and power routing on the two inner layers, to minimize noise pickup from adjacent boards. In SMT designs, make layers 2 & 4 AGND planes, and place as much routing as possible on layer 3, minimizing exposed routing on layer 1.

The AGND plane should completely underlie **all** analog circuitry, including and D/A or A/D converters or CODECs. There should be **no** VCC or GND routing, or unnecessary digital signal routing through the area covered by the AGND plane.

Analog Signal Routing

Proper component is essential to getting optimum audio performance. All traces should be kept as short and straight as possible. Avoid running traces parallel to other traces for other than very short distances. Keep any digital or clock traces as far as possible from A/D and D/A converters.

To minimize noise pickup, all routing to op-amp inputs should be kept as short as possible. Op-amp output signals are far less critical, being driven by a relatively low impedance source. Avoid routing op-amp input and output signals near each other to prevent feedback problems. Also, be sure to follow the supply bypassing guidelines below. never route an analog signal through a digital area, or vice-versa.

Audio Board Design & PCB Layout Guidelines(Continued)

Digital Signal Routing

Use of vias should be minimized, particularly on high speed signals, such as clocks. For this reason, hand-routing is **strongly** recommended, rather than using an auto-router. Even the auto-routers available today will use far more vias than an experienced hand-router. Our evaluation boards are all completely hand-routed. Keep all unbuffered PC-bus signals as short as possible, preferably no more than 1-2″. Also rigorously avoid passing digital signals over any splits in the planes. Keep all crystals as close as possible to the other components to which they are connected, and, if possible, surround their traces with GND traces. **Never** allow an oscillator or clock signal to cross the GND/AGND plane split! Securely attach, by soldering, the crystal case to its associated ground plane, usually GND.

Supply Bypassing

In the digital section of the board, be sure no VCC pin is more than about 1″ from a bypass capacitor. In the analog section, this may be relaxed somewhat, but try to ensure that each supply pin is within at least 1.5-2″ of a bypass capacitor. In both the digital and analog sections, evenly distribute the bypass capacitors, and use an even mix of 0.1μF and 0.001μF capacitors. For the KS0165, one bypass capacitor for each VCC pin is recommended. All bypass capacitors should be routed such that the connection is from the VCC and GND planes to the capacitor, and then from the capacitor to the IC pins.

EMI Suppression

Adequate EMI suppression can most easily be achieved through careful PCB layout, and the use of small capacitors to GND/AGND, rather than ferrite beads. Since the analog input and output signal points are all (relatively) low impedance, small capacitors(1-10nF) can be connected between these points and AGND with no appreciable effect on audio performance. All such capacitors should be places as close as possible to the connectors, and the traces leaving them (going to the connectors) should not pass near any unfiltered traces which might couple-in unwanted high-frequency noise.

PACKAGE DIMENSIONS (100-QFP-1420C)