GMM79256NS-70/80/10

262,144 WORDS×9 BIT
CMOS DYNAMIC RAM MODULE

Description

The GMM79256NS is a 256K×9 bits Dynamic RAM Module, mounted 2 pieces of 1M bit DRAM (GM71C4256ASJ, 256K×4) sealed in 20 pin SOJ package and a 256K bit DRAM (GM71C-256A, 256K×1) in 18 pin PLCC package. The GMM79256NS is a socket type memory module, suitable for easy interchange or addition of module. The GMM79256NS provides common data inputs and outputs, and also provides separate I/O on parity bit for parity check. It's module board has decoupling capacitors mounted under each DRAM.

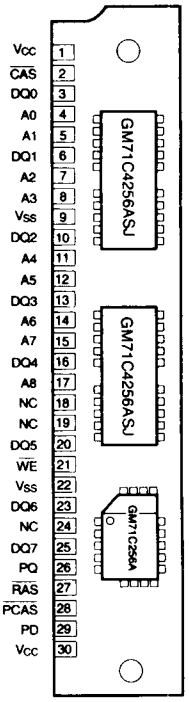
Features

- High Density Standard 30 pin mounting 2 pcs of 1M DRAM GM71C4256ASJ (SOJ) and a 256K DRAM GM71C256A(PLCC)
- Fast Page Mode Capability
- Single Power Supply
- Fast Access Time & Cycle Time (Unit : ns)

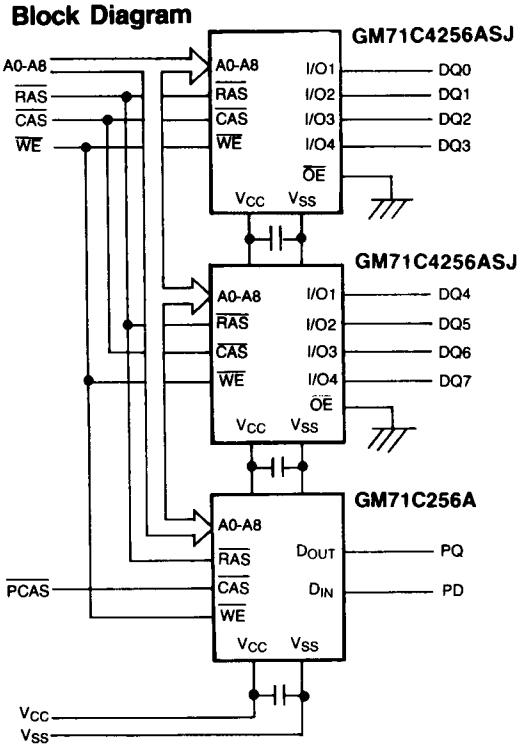
	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
GMM79256NS-70	70	20	130	50
GMM79256NS-80	80	25	160	55
GMM79256NS-10	100	25	190	60

- Low Power
  Active: 1,265/1,100/935mW (MAX)
  Standby: 27.5mW (CMOS level: MAX)
- $\overline{RAS}$ Only Refresh, $\overline{CAS}$ before $\overline{RAS}$ Refresh, Hidden Refresh Capability
- All inputs and outputs TTL Compatible
- 512 Refresh Cycles/8ms

Pin Configuration (Top View)



Block Diagram



Pin Description

Pin	Function	Pin	Function
A0~A8	Address	$\overline{WE}$	Read/Write Enable
DQ0~DQ7	Data Input/Data Output	PD	Data in for Parity
$\overline{RAS}$	Row Address Strobe	PQ	Data out for Parity
$\overline{CAS}$	Column Address Strobe	V_{SS}	Ground
$\overline{PCAS}$	$\overline{CAS}$ for Parity	V_{CC}	Power (+5V)
NC	No Connection		

Note: 1. Common $\overline{CAS}$ control for eight common data-in and data-out lines.
2. The common control for one separate pair of data-in and data-out lines.
3. The common I/O feature dictates the use of only early write operations to prevent contention on data-in and data-out.

Absolute Maximum Ratings*

Symbol	Parameter	Rating	Unit
T_A	Ambient Temperature under Bias	0~70	°C
T_{STG}	Storage Temperature	−55~125	°C
V_{IN}/V_{OUT}	Voltage on any Pin Relative to V_{SS}	−1.0~7.0	V
V_{CC}	Power Supply Voltage	−1.0~7.0	V
I_{OUT}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	3.0	W

*Note: Stress greater than above listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

Recommended Operating Conditions (T_A=0 ~ 70°C)

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.4	—	6.5	V	1
V_{IL}	Input Low Voltage	−1.0	—	0.8	V	1

Note: 1. All voltages referenced to V_{SS}

DC Electrical Characteristics: (V_{CC} = 5V ± 10%, T_A = 0 ~ 70°C)

Symbol	Parameter		Min	Max	Unit	Note
V_{OH}	Output Level Output "H" Level Voltage (I_{OUT} = −5mA)		2.4	V_{CC}	V	
V_{OL}	Output Level Output "L" Level Voltage (I_{OUT} = 4.2mA)		0	0.4	V	
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	70ns	—	230	mA	1,2
		80ns	—	200		
		100ns	—	170		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS}$ = V_{IH})		—	7.5	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min)	70ns	—	230	mA	2
		80ns	—	200		
		100ns	—	170		
I_{CC4}	Fast Page Mode Current Average Power Supply Current Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Address Cycling: t_{PC} = t_{PC} min)	70ns	—	185	mA	1,3
		80ns	—	160		
		100ns	—	130		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS}$ = V_{CC} − 0.2V)		—	5	mA	
I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ Refresh Current (t_{RC} = t_{RC} min)	70ns	—	210	mA	
		80ns	—	200		
		100ns	—	170		
I_{CC7}	Standby Current $\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{OUT} = Enable		—	14	mA	1
$I_{I(L)}$	Input Leakage Current Any Input (0V ≤ V_{IN} ≤ 7V) All other Pins Not Under Test = 0V	PD, $\overline{PCAS}$	−10	10	μA	
		ADDR., $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	−30	30		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is Disabled, 0V ≤ V_{OUT} ≤ 7V)		−10	10	μA	

Note: 1. I_{CC} depends on output loading condition when the device is selected. I_{CC} (max) is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}

Capacitance (V_{CC} = 5V ± 10%, T_A = 25°C, f = 1MHz)

Symbol	Parameter	Min	Max	Unit	Note
C_{I1}	Input Capacitance (Address)	–	30	pF	1
C_{I2}	Input Capacitance (Clocks)	–	36	pF	1,2
C_{I3}	Input Capacitance (PD)	–	10	pF	1
$C_{I/O}$	I/O Capacitance (DQ0 ~ DQ7)	–	17	pF	1,2
C_O	Output Capacitance (PQ)	–	10	pF	1,2

Note 1. Capacitance shall be measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{OUT}.

AC Electrical Characterstics (V_{CC} = 5V ± 10% T_A = 0 ~ 70°C, Note 1, 14)

The GMM79256NS writes data only in early write cycle (twcs ≥ twcs (min)).
Delayed write cycle is not available because of I/O common.

Read, Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	GMM79256NS-70		GMM79256NS-80		GMM79256NS-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	130	–	160	–	190	–	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	50	–	70	–	80	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10,000	80	10,000	100	10,000	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	25	10,000	25	10,000	ns	
t_{ASR}	Row Address Set-up Time	0	–	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	15	–	15	–	15	–	ns	
t_{ASC}	Column Address Set-up Time	0	–	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	15	–	20	–	20	–	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	25	55	25	75	ns	8
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	20	40	20	55	ns	9
t_{RSH}	$\overline{RAS}$ Hold Time	25	–	25	–	30	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70	–	80	–	100	–	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	15	–	15	–	15	–	ns	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t_{REF}	Refresh Period	–	8	–	8	–	8	ms	

Read Cycle

Symbol	Parameter	GMM79256NS-70		GMM79256NS-80		GMM79256NS-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	70	—	80	—	100	ns	2,3
t_{CAC}	Access Time from $\overline{CAS}$	—	20	—	25	—	25	ns	3,4
t_{AA}	Access Time from Column Address	—	35	—	40	—	45	ns	3,5
t_{RCS}	Read Command Set-up Time	0	—	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	0	—	ns	
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	10	—	10	—	10	—	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	—	40	—	45	—	ns	
t_{OFF}	Output Buffer Turn-off Delay Time	—	20	—	20	—	25	ns	6

Write Cycle

Symbol	Parameter	GMM79256NS-70		GMM79256NS-80		GMM79256NS-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{WCS}	Write Command Set-up Time	0	—	0	—	0	—	ns	10
t_{WCH}	Write Command Hold Time	15	—	20	—	20	—	ns	
t_{WP}	Write Command Pulse Width	15	—	15	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	—	25	—	25	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	—	25	—	25	—	ns	
t_{DS}	Data-in Set-up Time	0	—	0	—	0	—	ns	11
t_{DH}	Data-in Hold Time	15	—	20	—	20	—	ns	11

Refresh Cycle

Symbol	Parameter	GMM79256NS-70		GMM79256NS-80		GMM79256NS-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{CSR}	$\overline{CAS}$ Set-up Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	10	—	10	—	10	—	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	20	—	25	—	30	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	10	—	10	—	10	—	ns	

Fast Page Mode Cycle

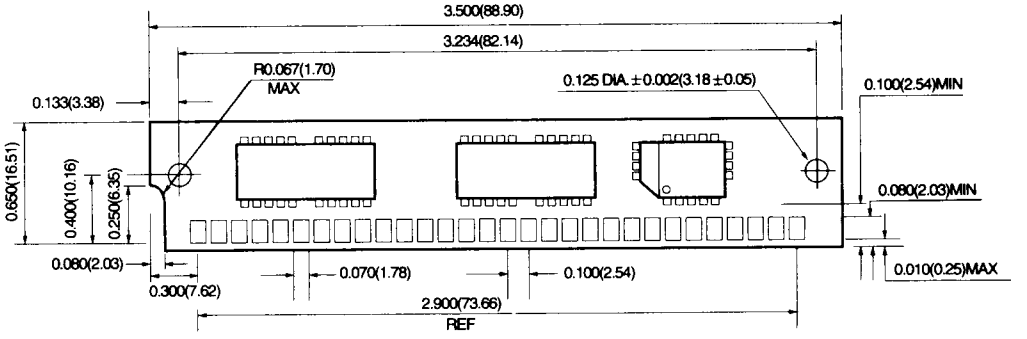
Symbol	Parameter	GMM79256NS-70		GMM79256NS-80		GMM79256NS-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{PC}	Fast-Page Mode Cycle Time	50	—	55	—	55	—	ns	
t_{CP}	Fast Page Mode $\overline{CAS}$ Precharge Time	10	—	15	—	20	—	ns	
t_{RASC}	Fast Page Mode $\overline{RAS}$ Pulse Width	—	100,000	—	100,000	—	100,000	ns	12
t_{ACP}	Access Time from $\overline{CAS}$ Precharge	—	45	—	50	—	55	ns	13
t_{RHCP}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	45	—	50	—	50	—	ns	

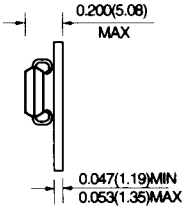
Notes :

1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leq t_{RCD}(max)$ and $t_{RAD} \leq t_{RAD}(max)$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100pF.
4. Assumes that $t_{RCD} \geq t_{RCD}(max)$ and $t_{RAD} \leq t_{RAD}(max)$.
5. Assumes that $t_{RCD} \leq t_{RCD}(max)$ and $t_{RAD} \geq t_{RAD}(max)$.
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Also transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS} is not restrictive operating parameters. It is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle.
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles.
12. t_{RASC} defines $\overline{RAS}$ pulse width in Fast Page Mode cycles.
13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
14. An initial pause of 100μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$ only refresh). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.

Package Dimensions

Unit: inches (mm)





Tolerance: ±0.005(0.13) unless otherwise specified.