Semiconductor Corporation

CS9203

Advanced Music Synthesizer

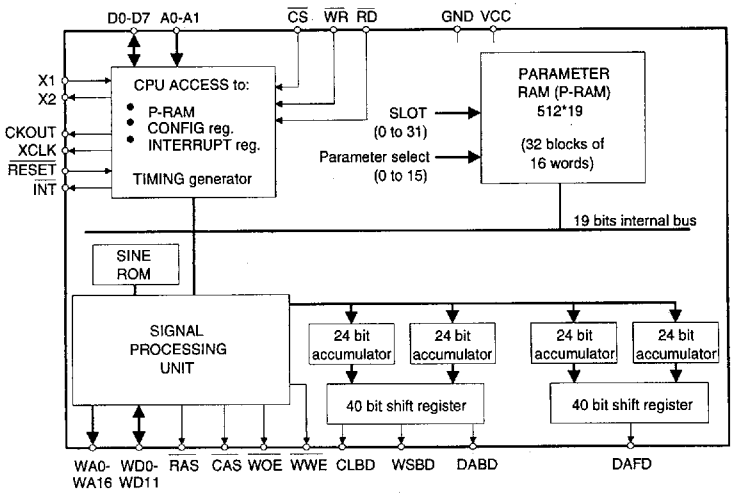
Features

- Polyphonic up to 32 notes
- Multi-timbral up to 32 simultaneous timbres
- 15 built-in synthesis algorithms
- On-chip high speed adder, multiplier, and 24 bit accumulators with overflow protection
- Built-in sine wave data
- Addresses up to 8Mx12 external sampling memory (ROM, SRAM, or DRAM)
- Two stereo 16 - 20 bit digital audio outputs (four audio outputs)
- Independent pan and volume mix assignable for each voice
- +5V supply CMOS, 50 mW power
- 68 pin PLCC package

General Description

The CS9203 is a high performance signal processor which is specially designed for high-quality music synthesis applications. Fifteen built-in music synthesis algorithms make the CS9203 extremely flexible, and the advanced features associated with it's PCM sampling algorithms, such as linear interpolation between samples, linear segment envelope generator, and 12 dB variable Q filtering, make the CS9203 a superb wave table synthesis engine. Dual stereo digital audio outputs are provided to allow the addition of an external effects processor, such as the CS8905. The 32 note polyphony and 32 part multi-timbral capabilities of the CS9203 make it an ideal choice for General MIDI (GM) synthesis applications, including musical instruments, MIDI sound modules, Karaoke machines, and high quality Personal Computer sound cards.

ORDERING INFORMATION
CS9203-CL 68-pin PLCC



Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
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ABSOLUTE MAXIMUM RATINGS (All voltages with respect to 0V, GND=0V)

Parameter	Symbol	Min	Typ	Max	Unit
Ambient Temperature (Power Applied)	-	-40	-	+85	°C
Storage Temperature	-	-65	-	+150	°C
Voltage on any Pin	-	-0.5	-	V_{CC}+0.5	V
Supply Voltage	V_{CC}	-0.5	-	6.5	V
Maximum I_{OL} Per I/O Pin	-	-	-	10	mA

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage	V_{CC}	4.75	-	5.25	V
Operating Ambient Temperature	T_A	0	-	70	°C

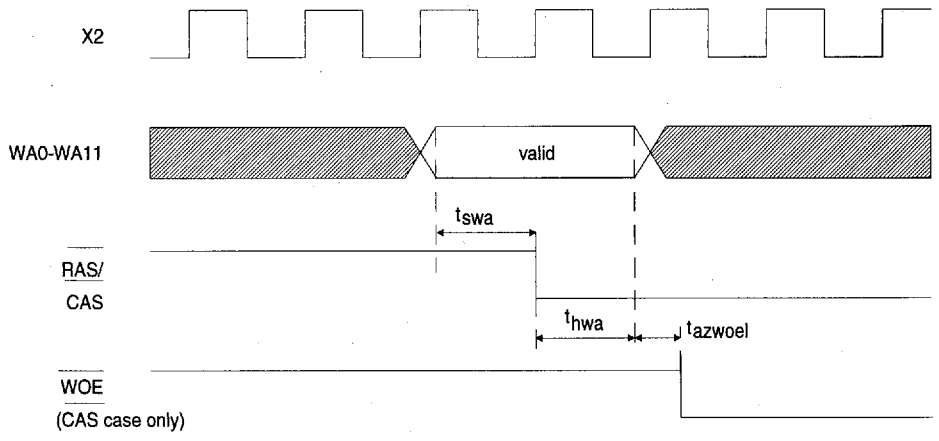
D.C. CHARACTERISTICS (T_A=25°C, V_{CC}=5V ±5%)

Parameter	Symbol	Min	Typ	Max	Unit
Low-Level Input Voltage	V_{IL}	-0.5	-	0.8	V
High-Level Input Voltage	V_{IH}	2.0	-	V_{CC}+0.5	V
Low-Level Output Voltage at I_{OL}=3.2 mA	V_{OL}	-	-	0.45	V
High-Level Output Voltage at I_{OH}=-0.8 mA	V_{OH}	2.4	-	-	V
Power Supply Current (Note 1) crystal frequency=50.000MHz	I_{CC}	-	10	25	mA

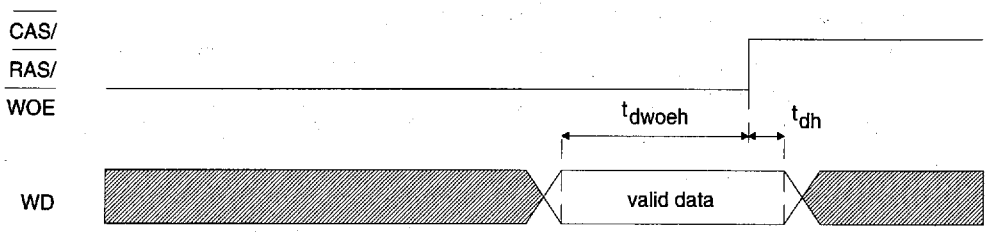
Notes: 1. Digital Inputs at Logic "1" = Vcc; Logic "0" = DGND, Power Supply Current does not include output loading

SWITCHING CHARACTERISTICS (T_A=25°C, V_{CC}=5V ±5%, Digital Inputs at Logic "1" = Vcc; Logic "0" = DGND, load capacitance=80pF for all outputs except X2)

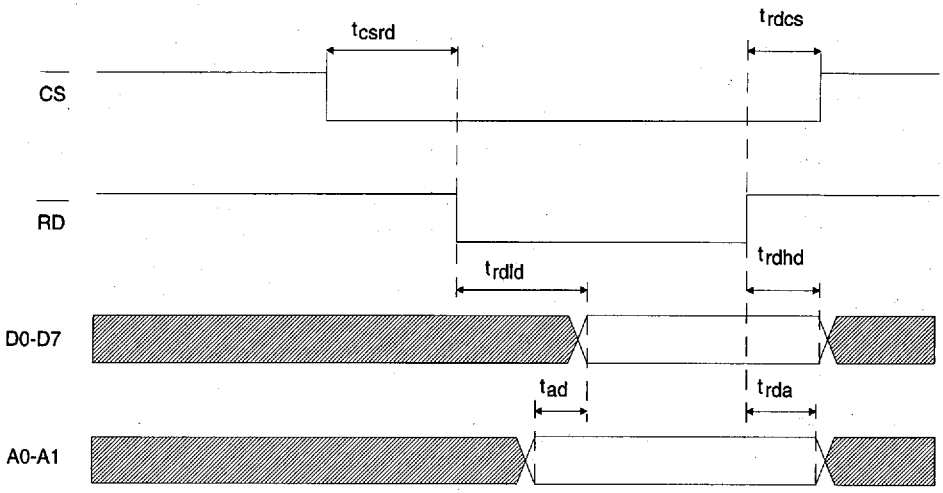
Parameter	Symbol	Min	Typ	Max	Unit
Oscillator Frequency	1/tclcl	0	48.0	50	MHz
$\overline{CS}$ Low to $\overline{WR}$ Low	tcswr	50	-	-	ns
$\overline{WR}$ High to $\overline{CS}$ High	twrcs	20	-	-	ns
A0-A1, D0-D7 Valid before Rising $\overline{WR}$	tadwr	20	-	-	ns
A0-A1, D0-D7 Valid after Rising $\overline{WR}$	twrad	0	-	-	ns
$\overline{WR}$ Pulse Width	twr	50	-	-	ns
$\overline{CS}$ Low to $\overline{RD}$ Low	tcsrd	50	-	-	ns
$\overline{RD}$ High to $\overline{CS}$ High	trdcs	20	-	-	ns
$\overline{RD}$ Active to Valid Data Out	trdld	-	-	50	ns
Data Out Hold from $\overline{RD}$	trdhd	10	-	-	ns
A0-A1 Valid to Valid Data Out	tad	-	-	50	ns
A0-A1 Hold from $\overline{RD}$	trda	10	-	-	ns
Recover from Control Write	trecover	34xtclcl+10	-	-	ns
CLBD Period	tclbd	-	34xtclcl	-	-
WA Valid before $\overline{RAS}$ or $\overline{CAS}$ H to L	tswa	tclcl-5	-	-	ns
WA Valid after $\overline{RAS}$ or $\overline{CAS}$ H to L	thwa	tclcl-5	-	-	ns
WD Floating to $\overline{WOE}$ Low	tazwoel	0	-	-	ns
Valid Data in to Rising $\overline{WOE}$	tdwoeh	40	-	-	ns
Data in Hold after Rising $\overline{WOE}$	tdh	0	-	-	ns



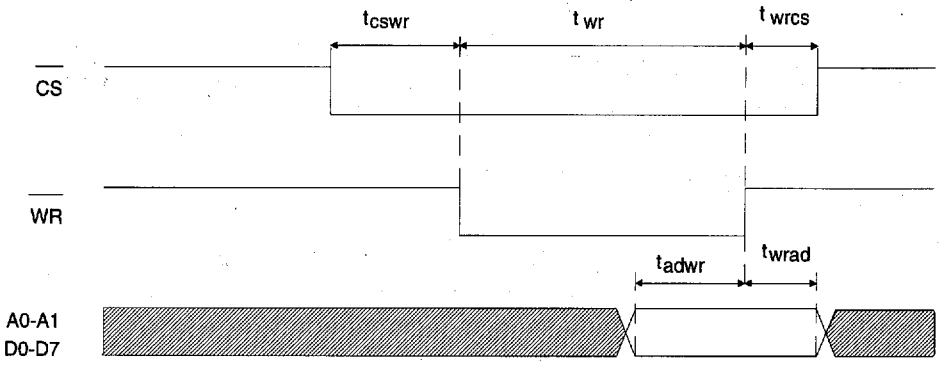
Sample Memory Address Timing



Sample Memory Data Bus Timing, Sample Memory Read



Microprocessor Read Cycle



Microprocessor Write Cycle

FUNCTIONAL DESCRIPTION

The CS9203 is a specialized high performance signal processor for music synthesis applications. The CS9203 signal processing unit includes a high speed adder, a multiplier, and specialized circuitry for phase computation, interpolation between samples, and amplitude envelope generation. The devices' internal data paths are 19 bits wide, and four 24-bit accumulators are used to generate the output samples for the four digital output channels of the device (two stereo output channels). The CS9203 has fifteen different built-in ROM-coded synthesis algorithms which can be used to generate a wide variety of sounds. A sixteenth algorithm is included for DRAM refresh in applications which store PCM sound samples in Dynamic RAM

The sample memory interface allows PCM sample-based synthesis algorithms to access sound samples stored off-chip in DRAM, SRAM, or ROM. Sine wave data is contained on-chip. An on-chip Parameter RAM (P-RAM) block provides RAM workspace for the synthesis algorithms. The CS9203 synthesis functions are controlled by an external microprocessor. Typical connections for a wavetable synthesis application are indicated in Figure 1.

The CS9203 operates on a synthesis frame timing basis. A stereo digital audio sample is output at the end of each synthesis frame. Thus the output sampling rate is the same as the synthesis frame rate. The synthesis frame is divided into a number of time slots, which are referred to as synthesis slots. One of the CS9203's 15 synthe-

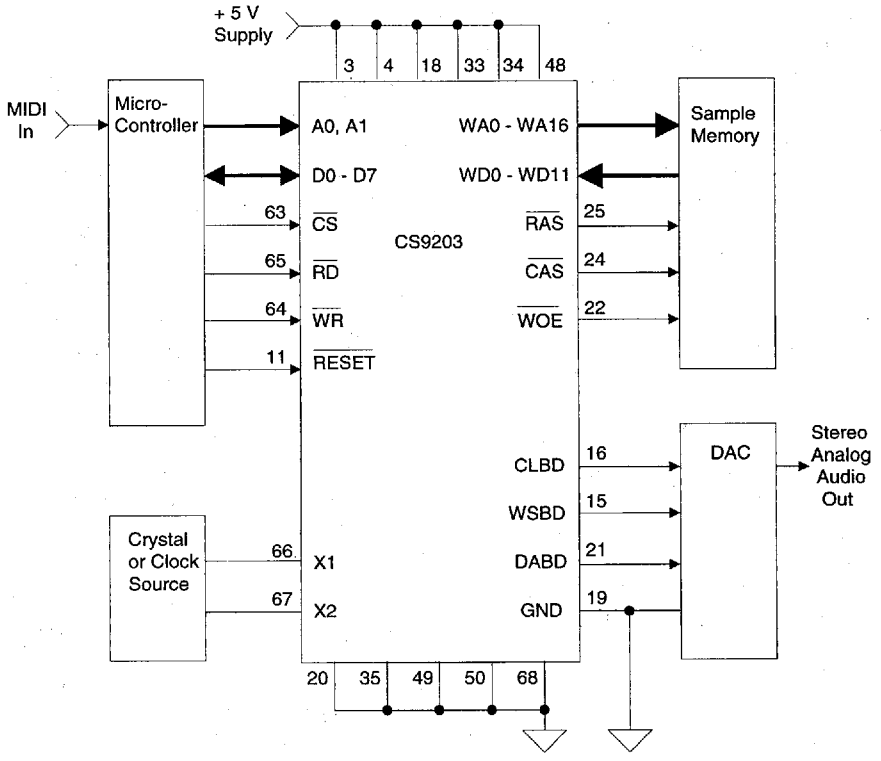


Figure 1. Typical Connection Diagram

sis algorithms is executed during each synthesis slot, and in general, each synthesis slot generates one note or voice. The number of synthesis slots in the synthesis frame can be set to any even number from 16 to 32. The length of a synthesis slot is 68 clock cycles (tclcl x 68), and the length of the frame is then (tclcl x 68 x N), where N is the number of synthesis slots per frame (N can be considered to be the number of notes of polyphony). The frame rate, or sampling rate, is the inverse of the frame length: Output Sampling Rate = 1/(tclcl x 68 x N) = Crystal Oscillator frequency/(68 x N) where N is the number of synthesis slots per frame.

The 512 x 19 bit Parameter RAM (P-RAM) is organized as 32 blocks of 16 words each. There is one 16 word x 19 bit block of Parameter RAM associated with each synthesis slot. The 16 word block of P-RAM associated with a particular slot holds all of the parameter data for that slot. The last word in the P-RAM block specifies which of the 16 built-in algorithms will be utilized for the synthesis slot. The specific data and format for the remaining 15 words of P-RAM in the block are algorithm dependent.

During each slot time, one algorithm is executed and the output sample from that algorithm is sent to the four 24-bit accumulators. The signal processing unit controls the level and balance of the output from the slot by scaling the sample output to the accumulators under the control of the mix parameters located in the P-RAM block for that slot. The accumulators are specially designed to prevent digital overflow. At the end of each frame, the contents of the accumulators are transferred to the four 20-bit output shift registers and the accumulators are cleared. The shift registers clock the resulting sample data out serially to the external Digital-to-Analog Converter(s).

Seven of the CS9203 synthesis algorithms utilize external PCM sound samples for high quality sound generation. Algorithm number 1, the High Quality Sampling algorithm, employs linear interpolation for frequency shifting, followed by a 12 dB variable-Q low-pass filter for timbre adjustment and elimination of noise which may be naturally created when transposing a samples' pitch during playback. The low-pass filter implementation has a variable cutoff frequency which may be controlled using a built-in envelope generator. A second envelope generator is utilized to control the final output amplitude for the resulting sound.

Other useful PCM sample-based algorithms include a 3X sampling algorithm for drums, a 2X sampling algorithm with 12 dB fixed-Q variable-cutoff low-pass filter, a 2X sampling algorithm with 12dB variable-Q variable-cutoff low-pass filter, a 1X sampling plus white noise algorithm with 12 dB variable-Q variable-cutoff low-pass filter, a 1X sampling algorithm with 24 dB variable-Q variable-cutoff low-pass filter, and an algorithm which combines a 1X pcm sampling operator with an algorithmic synthesis technique. The 3X sampling algorithm allows a single voice of polyphony (a single synthesis slot) to generate three simultaneous drum sounds. Separate envelope generators are used to control the output amplitude for each of the three sounds. The 2X sampling algorithm with 12 dB fixed-Q variable-cutoff low-pass filter is useful for generating "partials"-based sounds without the severe polyphony sacrifice normally associated with these techniques.

The remaining eight algorithms in the CS9203 employ algorithmic synthesis techniques which utilize the on-chip sine data rather than external PCM samples.

All of the PCM sample-based algorithms in the CS9203 support looped playback of samples. The sample memory address space is organized as 64 pages of 512 waves per page, where a wave is defined to be a block of 256 consecutive samples. A single sampled sound may occupy a maximum of one full page of sample memory

(128K samples). Three pointers are used to define the location of a sampled sound in memory. These pointers specify the Current Wave address, the End Wave address, and the Loop Wave address. Sample memory access during sound playback begins at the initial Current Wave address, and the current wave pointer is incremented during playback until the End Wave address is reached. The CS9203 supports two different loop modes for sound playback. In the more general case, when the current wave pointer value reaches the End Wave, it is automatically reloaded with the Loop Wave address. This mode of playback allows the lengths of the attack (non-looped) portion and the looped portion of the sampled sound to be optimized for the characteristics of that sound. In the "loop last wave" mode of operation, playback will always loop on the End Wave. One-shot sounds are implemented by including a blank wave at the end of the sound, and then utilizing the loop on last wave playback mode for the one-shot sound.

The pitch, or playback frequency, for playback of sampled sounds is specified by the 18 bit DPHI parameter. The upper 6 bits of the DPHI parameter are referred to as the upper phase bits, and these bits make up the six least significant bits of the sample memory address. The lower 12 bits of the DPHI parameter make up the fractional part of the phase. The frequency scaling on playback is equal to DPHI/4096. A DPHI value of 4096 (upper phase = 1, fractional part = 0) would play the samples from memory at the CS9203 output word rate. The fractional part of the phase is also used as the weighting constant for linear interpolation between samples when utilizing algorithm 1. A DPHI value of 2048 (upper phase = 0, fractional part = 2048) would play the samples from memory at one half the CS9203 word rate. In this case, every second value output from the algorithm would be an interpolated value to fill in the "missing point" midway between adjacent samples in memory.

Envelope generation in the CS9203 is of the linear segment type, allowing the creation of any piecewise linear envelope shape under external microprocessor control. The microprocessor specifies a rate of change and the amplitude endpoint for each segment, and the envelope generator will generate an interrupt to the microprocessor when the endpoint level has been reached.

Microprocessor Interface

The electrical interface between the microprocessor and the CS9203 is a standard bus interface, comprised of the address lines A0 and A1, the data lines D0-D7, the Chip Select signal $\overline{CS}$, the Write signal $\overline{WR}$, and the Read signal $\overline{RD}$. The external microprocessor controls the CS9203 synthesis functions by accessing the CS9203 Configuration Register, Interrupt Register, and Parameter RAM (P-RAM).

The Configuration Register is an 8-bit write-only control register which is comprised of the following control bits:

RUN	0 -	All slots are forced to idle mode, independent of the P-RAM contents (power-up default state).
	1 -	Synthesis slot processing is enabled as indicated by contents of the P-RAM.
OFST	0 -	The digital audio output data on DABD has no DC offset (power-up default).
	1 -	The digital audio output data on DABD includes a 5%positive DC offset.
IE	0 -	Envelope generator interrupts masked off (power-up default).
	1 -	Envelope generator interrupts enabled.
SFMT	0 -	Selects digital audio output format with idling on LSB (power-up default). See Figure 6.
	1 -	Selects digital audio output format with idling on MSB. See Figure 6.

S0 - S3 Slot Count Sequence - These 4 bits are used to select the number of synthesis slots to be used as follows:

S3	S2	S1	S0	No. Slots
1	X	X	X	16
0	0	0	0	18 (default)
0	0	0	1	20
0	0	1	0	22
0	0	1	1	24
0	1	0	0	26
0	1	0	1	28
0	1	1	0	30
0	1	1	1	32

The Control Register is accessed by first performing a Write operation to the CS9203 at Address A1A0 = 11 with data bit D6 =1 in order to set the CS9203 into the configuration mode. After setting the device to configuration mode, the configuration register data is written to address A1A0=00.

The Interrupt Register is an 8-bit read-only register which indicates the slot number and the envelope generator address within that slot which has caused the interrupt. The Interrupt Register is accessed by reading from the CS9203 at address A1A0 = 00.

The CS9203 Parameter RAM (P-RAM) is used to specify the synthesis algorithm and associated parameter data to be used for each synthesis slot. The P-RAM also functions as working RAM for the synthesis algorithm computations. There are 16 words of P-RAM associated with each synthesis slot. The P-RAM word size is 19 bits. The full address for a given P-RAM location is made up of a Page bit (P) and an 8-bit P-RAM address. The Page bit value is zero for parameters associated with slots 0 - 15, and one for slots 16-32. The 8-bit P-RAM address is comprised of a 4-bit Slot address and a 4-bit Parameter address (the 4-bit Parameter address identifies one parameter location in the 16-parameter block associated with the specified Slot). The parameter types, parameter data formats, and parameter addresses required for each slot depend on the specific synthesis algorithm being utilized for that slot. However, parameter location 15 in each 16-parameter block utilizes a common format which specifies the algorithm to be used for that slot, the output mix to be used, the phase angle constant (used by some algorithms), and the busy/idle status of the slot. Details of the sixteen synthesis algorithms and associated parameter data formats are not covered in this document. The P-RAM write sequence and P-RAM read sequence operations are indicated in Table 1 and Table 2.

Sample Memory Interface

The CS9203 can address up to 8 Msamples of external PCM sample memory. The 23-bit sample memory address is comprised of a 6-bit Page Address (PAGE0-PAGE5), a 9-bit Current Wave Address (CW0-CW8), and an 8-bit Upper Phase Address (PHI11-PHI18). This addressing technique organizes the sample memory into 64 pages, with each page containing 512 waves of 256 samples each. The Page Address bits (PAGE0-PAGE5), Current Wave Address bits (CW0-CW8), and Upper Phase Address bits (PHI11-PHI18) are output on the CS9203 Wave Address pins (WA0-WA11) in a time division multiplexed manner, using the $\overline{RAS}$ and $\overline{CAS}$ output signals as address strobes. Table 3 indicates the address bits which are available on the Wave Address signal pins (WA0-WA11) at $\overline{RAS}$ time, $\overline{CAS}$ time, and following the $\overline{CAS}$ strobe ($\overline{CAS}$+1 time). This memory addressing technique allows direct connection of large Dynamic RAMs with enable control inputs (x4 configurations). Large ROM memory configurations require external latches to capture a small subset of the address information on the Wave Address lines (WA9-WA11) during the $\overline{RAS}$ and $\overline{CAS}$ strobes. A typical external sampling memory read sequence is shown in Figure 2. Note that the cycle on which the $\overline{RAS}$ and $\overline{CAS}$ strobes occur is algorithm dependent.

Operation	Address A1	A0	Data D7	D6	D5	D4	D3	D2	D1	D0
Step 1. Select P-RAM Address Inside Page ($\overline{CS}$=$\overline{WR}$=0)	0	0	P-RAM Address (8bits)							
Step 2. Write Low data Byte ($\overline{CS}$=$\overline{WR}$=0)	0	1	B7	B6	B5	B4	B3	B2	B1	B0
Step 3. Write Mid Data Byte ($\overline{CS}$=$\overline{WR}$=0)	1	0	B15	B14	B13	B12	B11	B10	B9	B8
Step 4. Write High Data Bits, Select Page P and Request Write ($\overline{CS}$=$\overline{WR}$=0)	1	1	P	0	X	X	X	B18	B17	B16

Notes: 1. Allow 68 crystal clock cycles (1.36 µs @50MHz) between step 4 and subsequent step 1 or read operations.
2. Steps 2 and 3 can be omitted when writing repetitive data.
3. Steps 1, 2 and 3 can occur in any order.
4. The page P selected on step 4 remains valid for subsequent reads.

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Table 1. P-RAM Write Sequence

Operation	Address A1	A0	Data D7	D6	D5	D4	D3	D2	D1	D0
Step 1. Select P-RAM Page ($\overline{CS}$=$\overline{WR}$=0)	1	1	P	1	X	X	X	X	X	X
Step 2. Dummy Read ($\overline{CS}$=$\overline{RD}$=0)	0	1	X	X	X	X	X	X	X	X
Step 3. Select P-RAM Address in Page and Request Read ($\overline{CS}$=$\overline{WR}$=0)	0	0	P-RAM Address (8Bits)							
Step 4. Read Low Data Byte ($\overline{CS}$=$\overline{RD}$=0)	0	1	B7	B6	B5	B4	B3	B2	B1	B0
Step 5. Read Mid Data Byte ($\overline{CS}$=$\overline{RD}$=0)	1	0	B15	B14	B13	B12	B11	B10	B9	B8
Step 6. Read High Data Byte ($\overline{CS}$=$\overline{RD}$=0)	1	1	X	X	X	X	X	B18	B17	B16

Notes: 1. Steps 1 and 2 can be omitted if the page bit P is already loaded (from a previous read or write).
2. Step 1 loads the page bit P and sets the configuration mode, this requires a dummy read on step 2.
3. At least 68 crystal clock cycles (1.36 µs @50MHz) are required between step 3 and the subsequent step.
4. Steps 4 to 6 can occur in any order.
5. Steps 4 to 6 are optional.

Table 2. P-RAM Read Sequence

Time	WA11	WA10	WA9	WA8	WA7	WA6	WA5	WA4	WA3	WA2	WA1	WA0
($\overline{RAS}$)	WWE	PAGE2	PAGE1	PAGE0	PHI18	PHI17	PHI16	PHI15	PHI14	PHI13	PHI12	PHI11
($\overline{CAS}$)	PAGE5	PAGE4	PAGE3	CWF8	CWF7	CWF6	CWF5	CWF4	CWF3	CWF2	CWF1	CWF0
($\overline{CAS}$+1)	CWF3	CWF2	CWF1	CWF0	PHI18	PHI17	PHI16	PHI15	PHI14	PHI13	PHI12	PHI11

Note WA12-WA16 output the following during $\overline{RAS}$, $\overline{CAS}$, and $\overline{CAS}$+1:

WA16	WA15	WA14	WA13	WA12
CWF8	CWF7	CWF6	CWF5	CWF4

Table 3. Sample Memory Address Multiplexing on WA0 - WA11

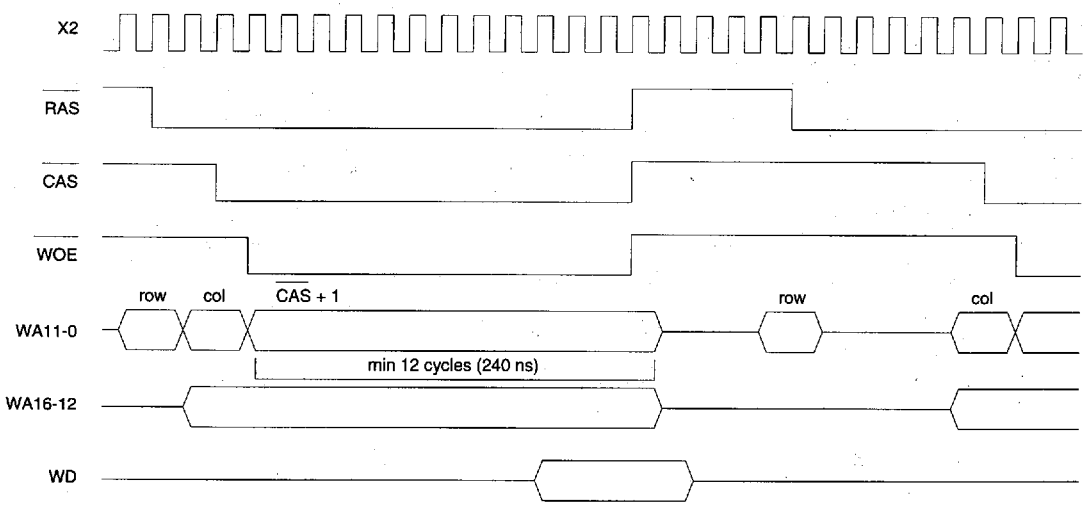

Figure 2. Typical External Memory Read Sequence

Figure 3 shows direct connection of three 4 Mbit (1Mx4) DRAM chips to form a 1Mx12 sample memory. Note that one synthesis slot can be assigned to algorithm number 16 to generate $\overline{RAS}$ before $\overline{CAS}$ refresh for Dynamic RAMs. The $\overline{CAS}$ before $\overline{RAS}$ refresh timing generated using algorithm 16 is shown in Figure 4. Note that algorithm 16 utilizes one of the synthesis slots, but this algorithm does not generate a voice. Thus, the polyphony of the CS9203 is reduced by one note when using Algorithm 16 to generate DRAM refresh.

DRAMs without enable control pins (x1 configurations) require the use of an external Flip-flop to capture the early write information (WWE) on the WA11 line at RAS time. DRAMs with static column mode access should not be used with the CS9203 because the addresses are not stable during the full CAS cycle.

Figure 5 shows the address latch circuitry required to address 8 Msamples of ROM memory. One 3-bit latch is clocked at RAS time to capture address lines WA17-WA19, the second 3-bit latch is clocked at $\overline{CAS}$ time to capture WA20-WA22. A 1Msample ROM implementation would require only the first 3-bit latch, a 128K sample ROM could be addressed directly by the CS9203.

DAC interface

The CS9203 DAC interface consists of a left/right clock signal WSBD, a bit clock CLBD and the stereo output data stream DABD or DAFD. The left/right clock signal WSBD and bit clock CLBD are common to both the main stereo serial data output DABD and the secondary stereo serial data output DAFD. The DAFD output is commonly used as a stereo effects send to an external effects processor, such as the CS8905. Two different serial DAC data formats are supported by the WSBD signal, as indicated in Figure 6. The serial DAC format is selected using the SFMT bit in the CS9203 Configuration Register. The number of data bits transmitted in the serial data output depends on the state of the SFMT bit, and on the number of synthesis slots being utilized as follows:

SFMT	Slots	Number of bits output
0	16	16
0	18	18
0	20-32	20
1	X	16

The number of bit clock (CLBD) cycles per frame is equal to two times the number of synthesis slots being used (two CLBD clock cycles per synthesis slot). When the number of synthesis slots used is larger than the number of output data bits, then the output data stream is padded with zeros as indicated in Figure 6. The most significant bit (MSB) of the left channel data is output during the slot 0 time, and the MSB of the right channel is output during the slot 8 time. The slot count sequence used in the CS9203 is represented in Figure 7. If 16 slots are utilized, the slot count sequence is straightforward (0,1, ... 15). If the slot count is greater than 16, then slots are added symmetrically after slot 7 and after slot 15. For example, if the number of slots is 20 (the number of slots is always an even number), then the slot count sequence will be (0, 1, ... 7, 16, 17, 8, 9, ... 15, 24, 25). In this case, slot numbers 18 - 23 and slot numbers 26 - 31 are not used. This allows the zero padding to be symmetrical with respect to the left channel and right channel data.

The ground reference for the DAC should be connected directly to the CS9203 GND at pin 19, and this should be the only connection between analog ground and digital ground.

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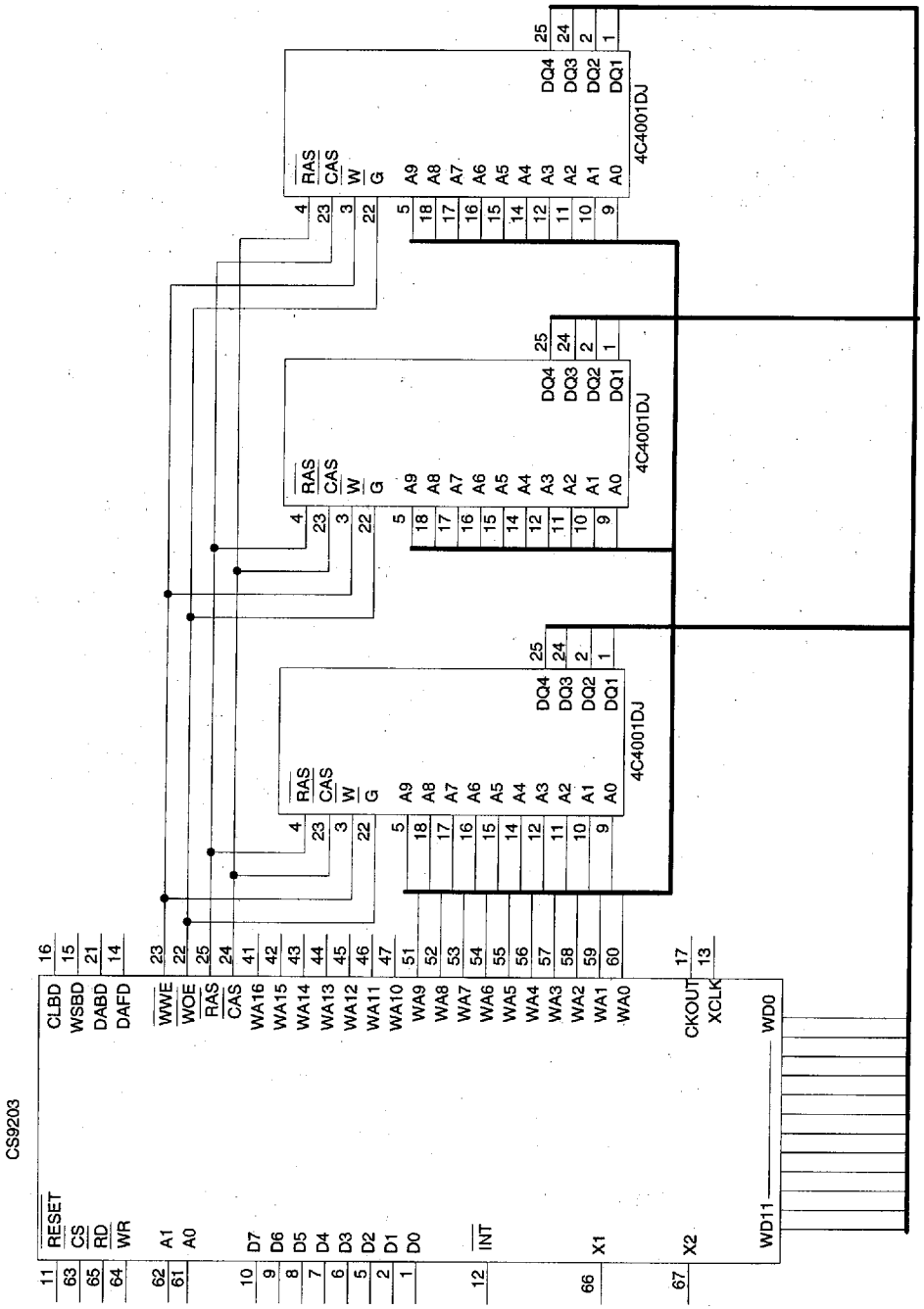


Figure 3. Direct Connection of 1M x 12 DRAM Sample Memory

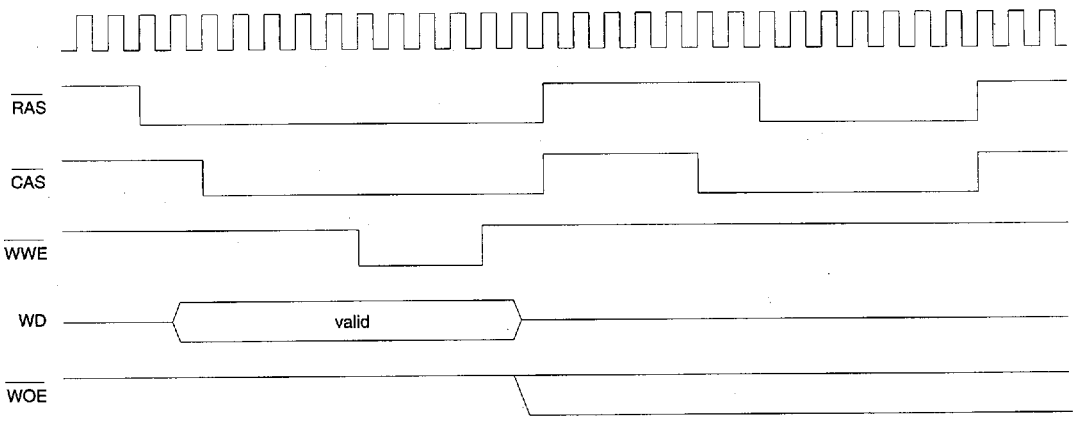


Figure 4. Algorithm 15, External RAM Write, $\overline{CAS}$ Before $\overline{RAS}$ Refresh

Oscillator Circuit

The CS9203 timing may be generated using the built-in crystal oscillator (external crystal circuit) or an external oscillator. Connections for a typical 3rd overtone series-resonant crystal oscillator circuit are shown in Figure 8. Trace lengths should be kept to a minimum, and the board layout should include ground plane beneath the oscillator circuit components.

If an external oscillator circuit in utilized, shield the input trace connecting the oscillator output to the X1 input at pin 66, and keep the trace lengths to a minimum. The ground for the oscillator circuit should be a direct connection to the CS9203 GND at pin 68.

CLKOUT and XCLK Clock Outputs

The frequency of the CKOUT output is the crystal oscillator frequency divided by four. The CKOUT output is disabled while the $\overline{RESET}$ input is low.

The XCLK output is a gated clock output which provides either 1024 or 2048 output clock pulses per synthesis frame. The period of the XCLK output pulses are the same as those of the CS9203 crystal oscillator. If the number of synthesis slots in use is less than 32, then the XCLK signal will output 64 pulses per synthesis frame for the first 16 synthesis frames executed, and then remain inactive for the balance of the frames. If the number of slots is equal to 32, then the XCLK signal will output 64 pulses dur-

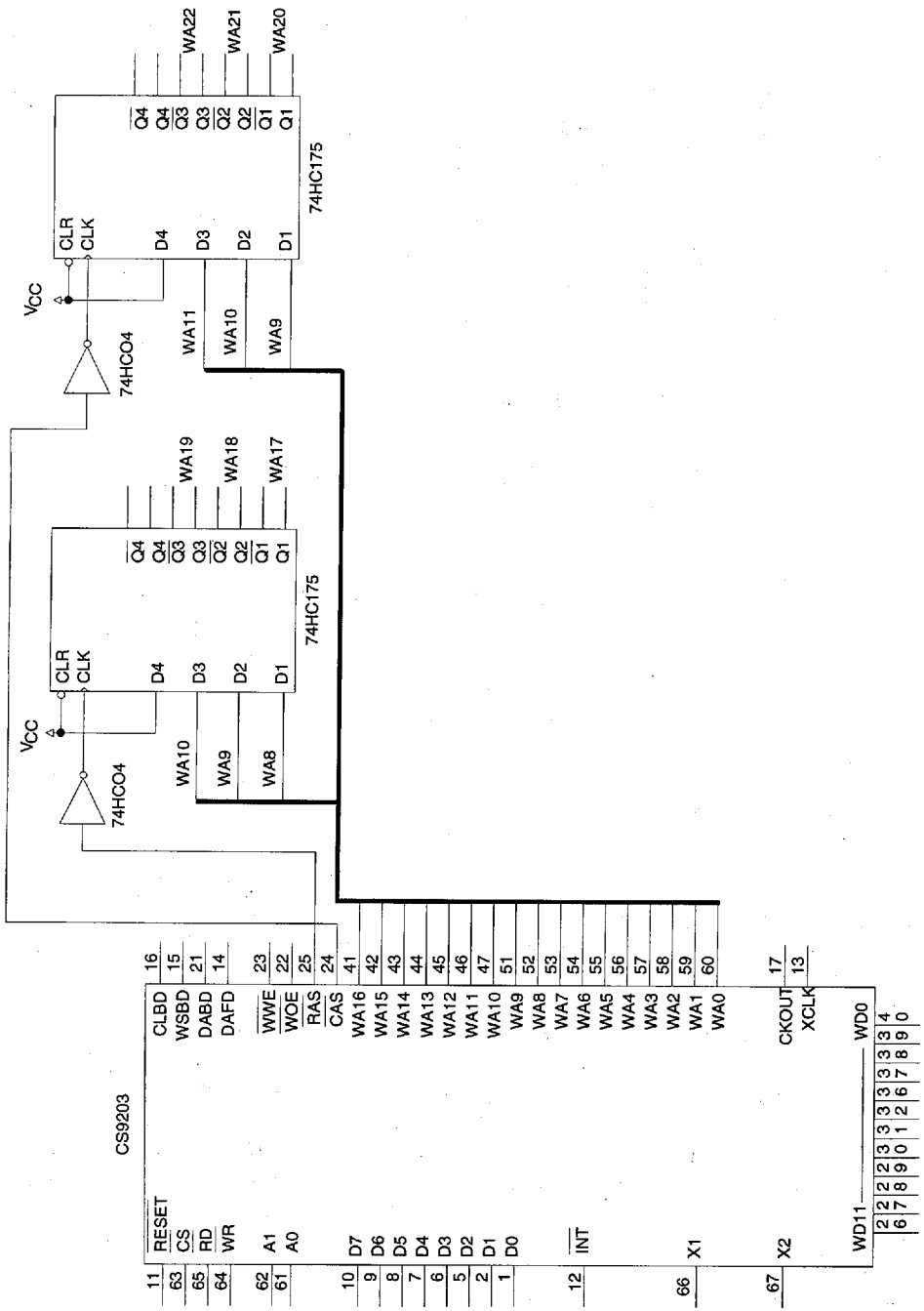


Figure 5. Address Generation for 8 Msample ROM Memory

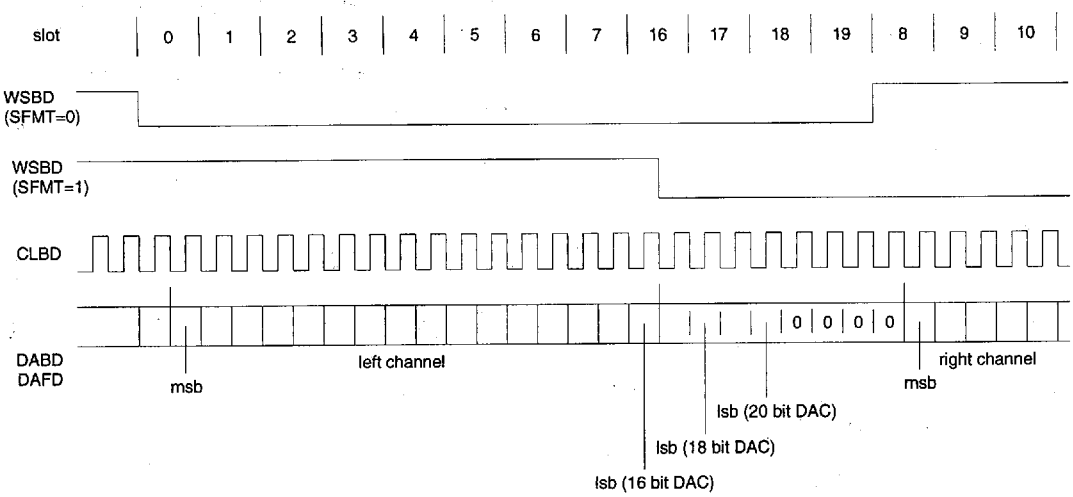


Figure 6. Typical Digital Audio Transfer Sequence (24 slots example, S3S2S1S0=1011)

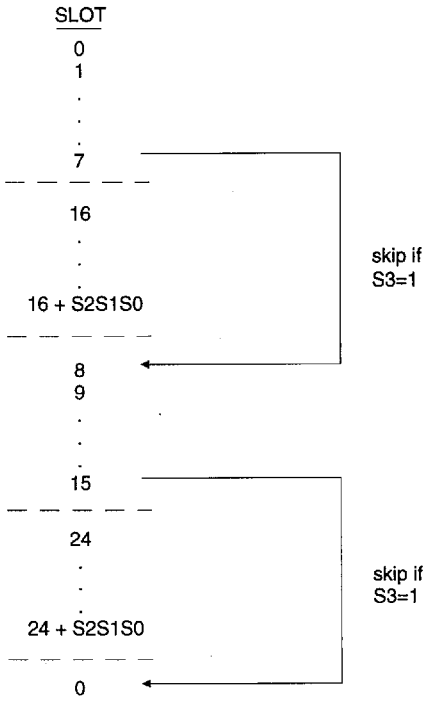


Figure 7. Slot Count Sequence

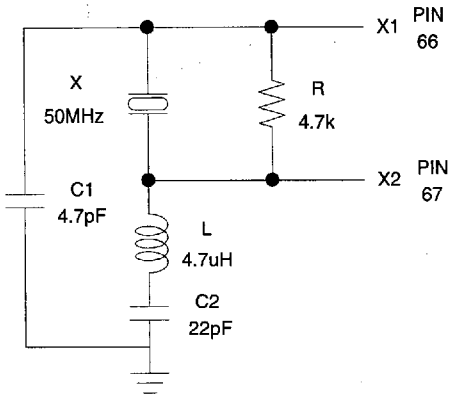


Figure 8. Typical Crystal Oscillator Component Connection

ing each of the 32 synthesis frames. Note that there are 68 crystal oscillator cycles per synthesis frame, and the XCLK output is gated 64 cycles on and 4 cycles off during each synthesis slot for which it is active. The XCLK output may be used to provide a clock input to a CS8905 when this device is used as an effects processor. The XCLK output is enabled during $\overline{\text{RESET}}$.

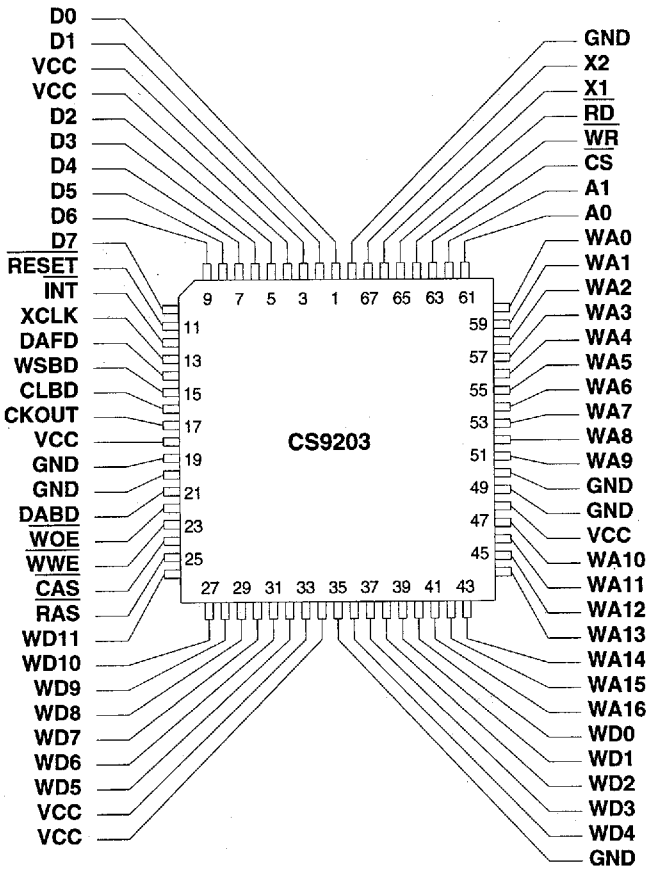
Power Connections and Decoupling

All power and ground pins on the CS9203 device should be connected to the appropriate supply planes using the shortest trace lengths possible. Recommended decoupling consists of four 0.1µF ceramic decoupling capacitors between V_{CC} and GND, one at each of the four sides of the IC. These capacitors should be placed as close to the IC as possible. In addition, place one 10µF Tantalum capacitor from V_{CC} at pin 3 to GND at pin 68 with minimum trace and lead lengths.

Power-up Reset

The $\overline{\text{RESET}}$ input must be held low until the oscillator circuit has stabilized. The CS9203 internal oscillator and the XCLK output signal are enabled during $\overline{\text{RESET}}$, other functions of the device are held in an idle mode while $\overline{\text{RESET}}$ is low.

PIN DESCRIPTIONS



Pins

D0-D7 - Bi-directional data bus to/from uP. Input/Output. PINS 1, 2, 5, 6, 7, 8, 9, and 10.
These bidirectional data lines are used to transfer data between an external microprocessor and the CS9203.

A0 and A1 - Address Bus Input from uP. PINS 61 and 62.
These pins allow an external microprocessor to select the CS9203 control register or specific data registers for read/write operations.

$\overline{CS}$ - Chip Select Input. PIN 63.
This is the CS9203 chip select input from an external microprocessor. Active low.

$\overline{WR}$ - Write to Chip Input. PIN 64.

This signal is the write strobe input to the CS9203 from an external microprocessor. This strobe is used to write to the CS9203. Active low.

$\overline{RD}$ - Read from Chip Input. PIN 65.

This signal is the read strobe input to the CS9203 from an external microprocessor. This strobe is used to read data from the CS9203. Active low.

$\overline{INT}$ - End of Envelope Interrupt Output. PIN 12.

This signal is an interrupt output from the CS9203 to an external microprocessor. Active low.

$\overline{RESET}$ - Chip Reset Input. PIN 11.

This active low input to the CS9203 is used to reset and initialize the CS9203. Active low.

X1 - Xtal Oscillator Input. PIN 66.

This signal is the input for the internal oscillator. A maximum crystal frequency of 50 MHz is supported. An external oscillator clock output signal may be connected at this pin.

X2 - Xtal Oscillator Output. PIN 67.

This signal is the internal oscillator output.

CKOUT - Clock Output. PIN 17.

This signal is an output clock. The clock frequency is the CS9203 oscillator frequency divided by four.

XCLK - External Effect Processor Clock Output. PIN 13.

This is a gated clock output. The clock period is the same as that of the CS9203 oscillator. If the number of synthesis slots being used is less than 32, then 1024 pulses will be output per synthesis frame. If 32 slots are programmed, then 2048 pulses will be output per frame.

WA0-WA16 - Multiplexed External Memory Address Output. PINS 60, 59, 58, 57, 56, 55, 54, 53, 52, 51, 47, 46, 45, 44, 43, 42, and 41.

These output address lines are used to address external sample memory.

WD0-WD11 - External Memory Data Input/Output. PINS 40, 39, 38, 37, 36, 32, 31, 30, 29, 28, 27, and 26

These bidirectional data lines are used to pass sample data between the CS9203 and external sample memory.

$\overline{CAS}$ - WA0-WA11 Column Address Strobe Output. PIN 24.

This memory address strobe output is used in conjunction with the multiplexed address output lines WA0-WA16.

$\overline{RAS}$ - WA0-WA11 Row Address Strobe Output. PIN 25.

This memory address strobe output is used in conjunction with the multiplexed address output lines WA0-WA16.

$\overline{\text{WOE}}$ - External memory Data Output Enable. PIN 22.
This signal is an output enable for external sample memory.

$\overline{\text{WWE}}$ - External Memory Write Output. PIN 23.
This signal is a write enable strobe for external sample memory.

CLBD - External DAC/Effect Serial Clock Output. PIN 16.
This signal is the bit clock for the CS9203 stereo serial digital audio outputs DABD and DAFD.

DABD - External DAC Serial Data Output. PIN 21.
This is the primary stereo serial digital audio output from the CS9203.

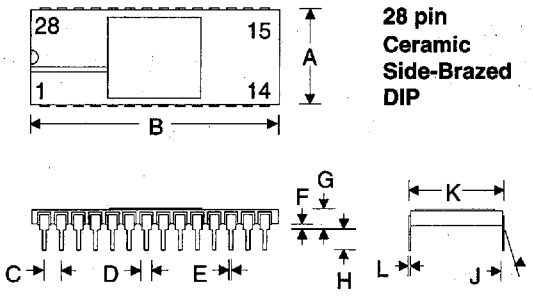
DAFD - External Effect Serial Data Output. PIN 14.
This is the secondary stereo digital audio output from the CS9203. This output is commonly used as an effects send to an outboard digital effects processor such as the CS8905.

WSBD - External DAC Effect Right/Left Channel Output. PIN 15.
This signal is the left/right word clock for the DABD and DAFD stereo digital audio outputs of the CS9203.

GND - Power Ground. PINS 19, 20, 35, 49, 50, and 68.
Ground pins. All ground pins should be connected to a low impedance ground plane.

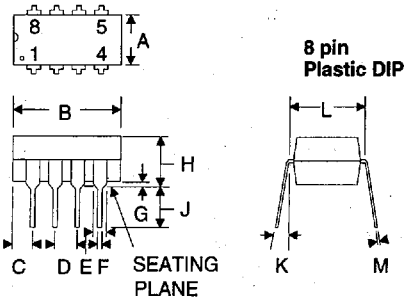
VCC - Power +5V, ±5%. PINS 3, 4, 18, 33, 34, and 48.
+5V power input pins. All V_{CC} pins should be connected to a low impedance +5V supply.

MECHANICAL DATA



28 pin Ceramic Side-Brazed DIP

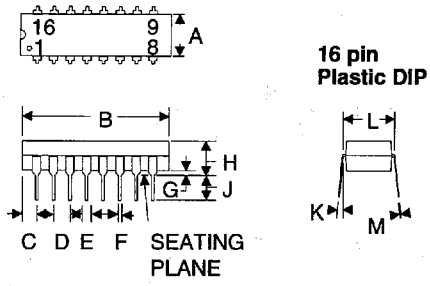
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.73	15.34	0.580	0.604
B	35.20	35.92	1.386	1.414
C	2.54 BSC		0.100 BSC	
D	0.76	1.40	0.030	0.055
E	0.38	0.53	0.015	0.021
F	1.02	1.52	0.040	0.060
G	2.79	4.32	0.110	0.170
H	2.54	4.57	0.100	0.180
J	-	10°	-	10°
K	14.99	15.49	0.590	0.610
L	0.20	0.30	0.008	0.012



8 pin Plastic DIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.60	0.240	0.260
B	9.14	10.2	0.360	0.400
C	0.38	1.52	0.015	0.060
D	2.54 BSC		0.100 BSC	
E	1.02	1.78	0.040	0.070
F	0.38	0.53	0.015	0.021
G	0.51	1.02	0.020	0.040
H	3.81	5.08	0.150	0.200
J	2.92	3.43	0.115	0.135
K	0°	10°	0°	10°
L	7.62BSC		0.300BSC	
M	0.20	0.38	0.008	0.015

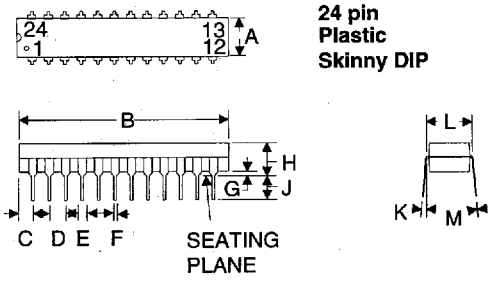
NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.13MM (0.005") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.



16 pin Plastic DIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.60	0.240	0.260
B	18.80	19.30	0.740	0.760
C	1.32	2.89	0.015	0.035
D	2.54 BSC		0.100 BSC	
E	1.02	1.78	0.040	0.070
F	0.38	0.53	0.015	0.021
G	0.51	1.02	0.020	0.040
H	3.81	5.08	0.150	0.200
J	2.92	3.43	0.115	0.135
K	0°	10°	0°	10°
L	7.62BSC		0.300BSC	
M	0.20	0.38	0.008	0.015

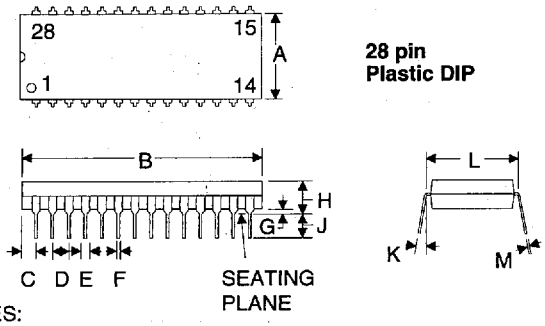
NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.13MM (0.005") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.



24 pin
Plastic
Skinny DIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.60	0.240	0.260
B	31.37	32.13	1.235	1.265
C	1.65	2.16	0.065	0.085
D	2.54 BSC		0.100 BSC	
E	1.02	1.52	0.040	0.060
F	0.36	0.56	0.014	0.022
G	0.51	1.02	0.020	0.040
H	3.94	4.57	0.155	0.180
J	2.92	3.43	0.115	0.135
K	0°	15°	0°	15°
L	7.62 BSC		0.300 BSC	
M	0.20	0.38	0.008	0.015

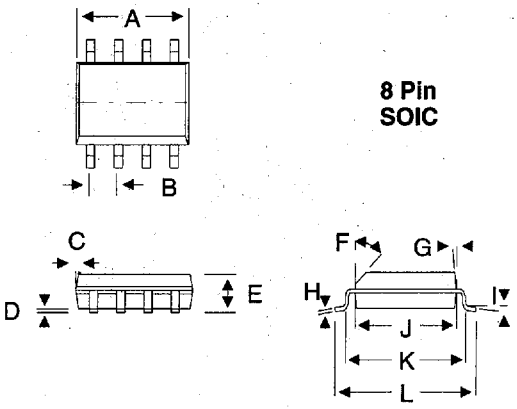
NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.25MM (0.010") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.



28 pin
Plastic DIP

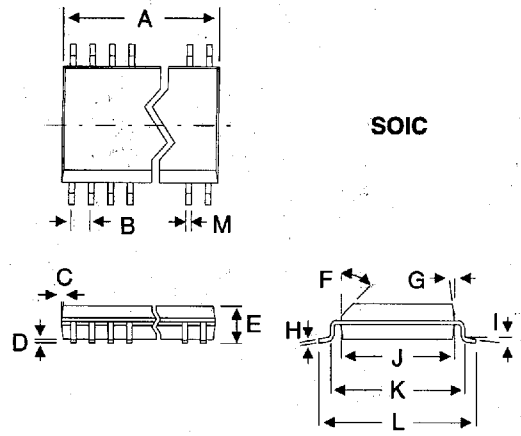
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	13.72	14.22	0.540	0.560
B	36.45	37.21	1.435	1.465
C	1.65	2.16	0.065	0.085
D	2.54 BSC		0.100 BSC	
E	1.02	1.52	0.040	0.060
F	0.36	0.56	0.014	0.022
G	0.51	1.02	0.020	0.040
H	3.94	5.08	0.155	0.200
J	2.92	3.43	0.115	0.135
K	0°	15°	0°	15°
L	15.24 BSC		0.600 BSC	
M	0.20	0.38	0.008	0.015

NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.25MM (0.010") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.



8 Pin SOIC

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.25	5.30	0.207	0.209
B	1.27 TYP		0.050 TYP	
C	7° NOM		7° NOM	
D	0.120	0.180	0.005	0.007
E	1.80	1.86	0.071	0.073
F	45° NOM		45° NOM	
G	7° NOM		7° NOM	
H	0.195	0.205	0.0078	0.0082
I	2°	4°	2°	4°
J	-	-	-	-
K	6.57	6.63	0.259	0.261
L	7.85	7.95	0.308	0.312

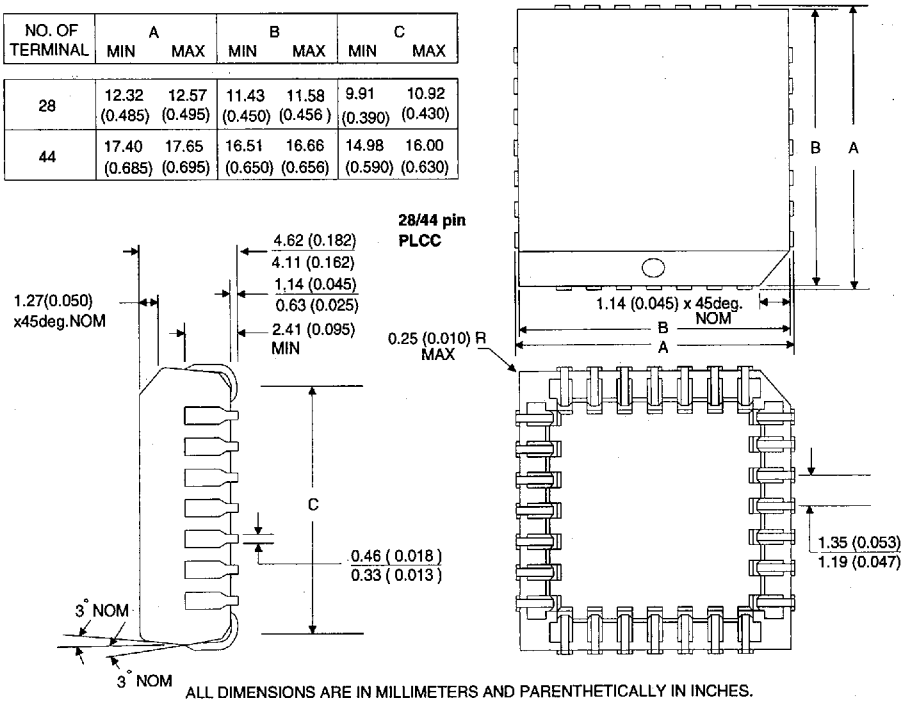


SOIC

pins	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
16	9.91	10.41	0.390	0.410
20	12.45	12.95	0.490	0.510
24	14.99	15.50	0.590	0.610
28	17.53	18.03	0.690	0.710

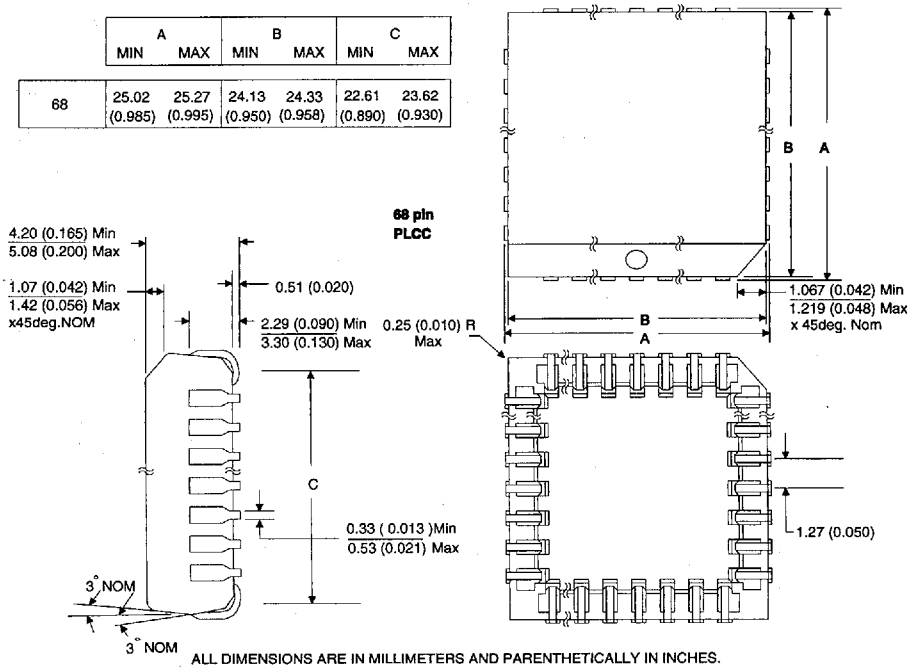
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	see table above			
B	1.27	BSC	0.050	BSC
C	7°	NOM	7°	NOM
D	0.127	0.330	0.005	0.013
E	2.41	2.67	0.095	0.105
F	45°	NOM	45°	NOM
G	7°	NOM	7°	NOM
H	0.203	0.381	0.008	0.015
I	2°	8°	2°	8°
J	7.42	7.59	0.292	0.298
K	8.76	9.02	0.345	0.355
L	10.16	10.67	0.400	0.420
M	0.33	0.51	0.013	0.020

NO. OF TERMINAL	A MIN	A MAX	B MIN	B MAX	C MIN	C MAX
28	12.32 (0.485)	12.57 (0.495)	11.43 (0.450)	11.58 (0.456)	9.91 (0.390)	10.92 (0.430)
44	17.40 (0.685)	17.65 (0.695)	16.51 (0.650)	16.66 (0.656)	14.98 (0.590)	16.00 (0.630)



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

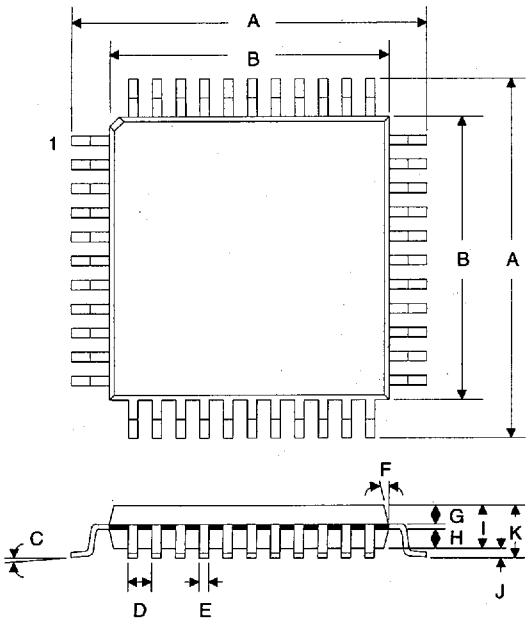
	A MIN	A MAX	B MIN	B MAX	C MIN	C MAX
68	25.02 (0.985)	25.27 (0.995)	24.13 (0.950)	24.33 (0.958)	22.61 (0.890)	23.62 (0.930)



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

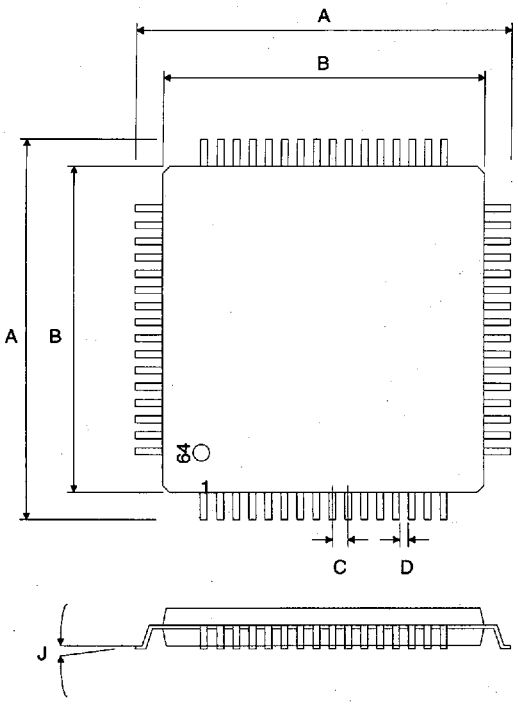
11

44 PIN QUAD FLATPACK



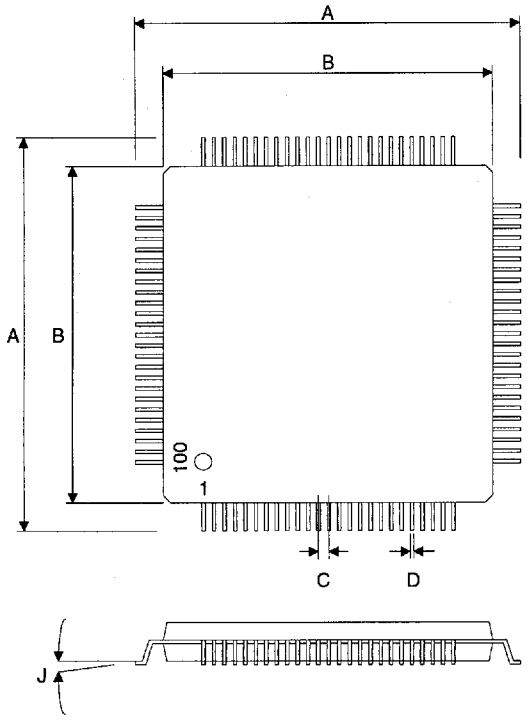
	44 Pin TQFP 1.4 mm Package Thickness			
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	11.75	12.25	0.463	0.482
B	9.90	10.10	0.390	0.398
C	0°	7°	0°	7°
D	0.80 BSC		0.031 BSC	
E	0.35 BSC		0.014 BSC	
F		12°		12°
G	0.54	0.74	0.021	0.029
H	0.54	0.74	0.021	0.029
I	1.35	1.50	0.053	0.059
J	0.05		0.002	
K		1.60		0.063
L		0.17		0.007
M	2°	10°	2°	10°
N	0.35	0.65	0.014	0.026

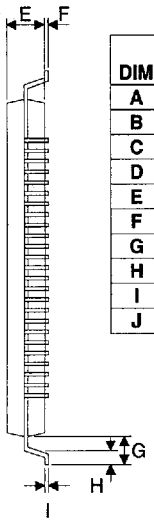
0.102 MAX
Lead Coplanarity



64 Pin TQFP

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.00 BSC		0.472 BSC	
B	10.00 BSC		0.393 BSC	
C	0.50 BSC		0.020 BSC	
D	0.14	0.30	0.005	0.012
E	0.95	1.12	0.037	0.044
F	0.05	0.15	0.002	0.006
G	1.00 BSC		0.039 BSC	
H	0.45	0.75	0.018	0.030
I	0.09	0.18	0.003	0.007
J	0°	7°	0°	7°





100-pin TQFP

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	15.75	16.25	0.620	0.640
B	13.90	14.10	0.547	0.555
C	0.50 BSC		0.020 BSC	
D	0.10	0.20	0.004	0.012
E	1.25	1.55	0.049	0.061
F	0.00	0.20	0.000	0.008
G	1.00 BSC		0.039 BSC	
H	0.35	0.65	0.014	0.026
I	0.077	0.177	0.003	0.007
J	0°	10°	0°	10°

11